30 Gb/s Direct Modulation of Holey VCSELs with Thermoelectric Cooling

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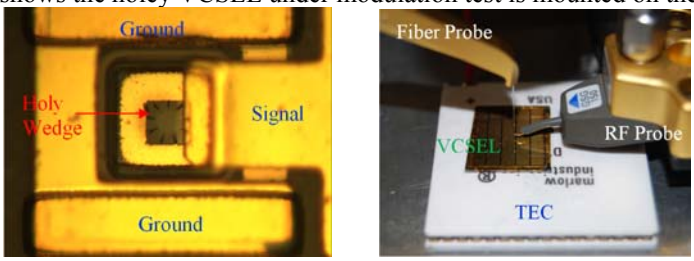
Abstract: We demonstrate a 25 Gb/s error-free operation of a directly modulated holey VCSEL, and the data rate can be extended to above 30 Gb/s when the VCSEL substrate temperature is stabilized by a thermoelectric cooler.

OCIS Codes: (142.7260) Vertical cavity surface emitting lasers (060.4080) Modulation (140.9560) Semiconductor lasers

High-speed modulation of VCSELs is desired for various applications, such as data communications and optical sensing. The highest data rate of a VCSEL achieved is 35 Gb/s using a tapered-oxide structure and operating at the 980-nm wavelength [1]. Micro thermoelectric coolers (TEC) are often incorporated into a VCSEL package to stabilize or tune the laser wavelength [2]. In this work, we demonstrate that the TEC can offer additional benefit to improve VCSEL operation data rates, offering a new perspective on VCSEL packaging for high-speed applications. Specifically, we demonstrate a 25 Gb/s error-free operation of a holey VCSEL at room temperature; when combined with the TEC, the error-free operation data rate can be extended above 30 Gb/s. We also measure the bit error ratio (BER) for a back-to-back transmission at three different data rates above 30 Gb/s and with different TEC currents.

The VCSEL used in this work is an 850-nm implant-confined holey VCSEL, and it was fabricated from a conventional epitaxy wafer and using a standard ion implantation process [3]. The holey pattern etched into the top distributed feedback reflector of the VCSEL increases the index guiding for the transverse optical modes, improving the laser efficiency and modulation bandwidth [3-4]. Fig. 1(a) shows a top view of the holey VCSEL. This particular holey pattern has a wedge structure [5], where it has the optical aperture diameter of 8 μm, the wedge number of 9 and the wedge angle of 20°. The ion implantation aperture diameter is 10 μm. A 40 ×40 mm^2 TEC is used to stabilize the substrate temperature of the holey VCSEL. Fig. 1 (b) shows the holey VCSEL under modulation test is mounted on the TEC surface.



(a) (b)

Fig. 1: (a) Optical image of the holey VCSEL and (b) VCSEL with TEC test setup in our experiment.

Fig.2 (a) compares the light-current-voltage (LIV) characteristics when the TEC current is 0 A and 1 A. The temperature of the cool side of the TEC decreases linearly from 25 °C (room temperature) to 5 °C, as the TEC current increases from 0 A (0 V) to 1 A (2.8 V). Note that water vapor forms on the VCSEL surface with the TEC current greater than 1 A, limiting the lowest substrate temperature used in our experiment to 5 °C. When the VCSEL substrate is held at 5 °C (1 A TEC current), the threshold of the VCSEL slightly decreases, the slope efficiency (between 3 and 12 mA) increases, and the maximum output light power also increase from 1.8 mW to 3 mW as compared to its characteristics at room temperature. The improved LI characteristic at a lower temperature is due to the increasing laser gain as expected. Fig. 2 (b) illustrates the optical spectrum taken at 13 mA dc current which is used later for high-speed modulation. Two dominate transverse modes are observed due to increased index guiding from the etched holey structure. The discontinuity in the LI curves at 13.1 mA indicates the sudden onset of a higher transverse mode, which may be due to the increasing thermal lensing [5]. The optical spectrum shifts to a shorter wavelength by 1.01 nm, when the TEC current varies from 0 A to 1 A. With the temperature change of

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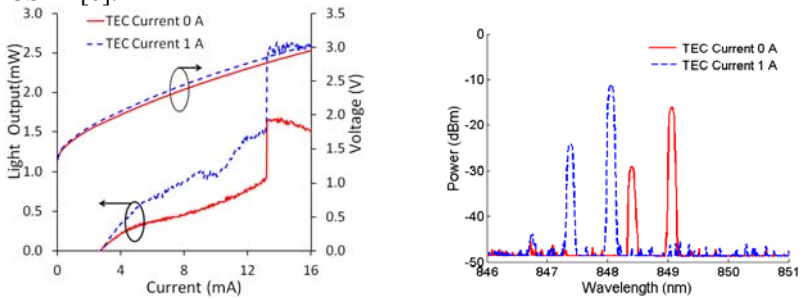
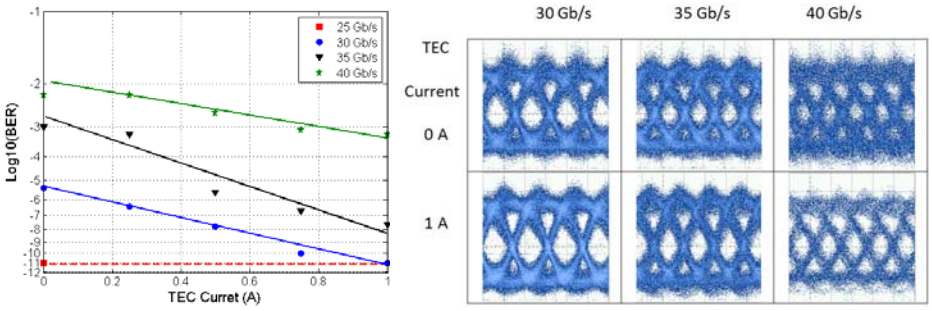
20 °C from the TEC, this wavelength shift is consistent with the cavity resonance shift of 0.06 nm/ °C for an 850-nm GaAs VCSEL [6].



(a) (b)

Fig. 2: (a) LIV characteristics and (b) optical spectrum of the holey VCSEL when the TEC currents are 0 A and 1 A.



(a) (b)

Fig. 3: (a) Different data rate BER at TEC current from 0 A to 1 A (Note: for 25 Gb/s, BER reaches the bottom line of the test system) (b) Eye diagrams at TEC current of 0 A (left) and 1 A (right), dimension: horizontal 20 ps/div, vertical 28.4 mV/div.

For high-speed experiment, the holey VCSEL is biased at 13 mA, and the peak-peak modulation voltage is 1 V. A 50 μm core multimode fiber is applied to couple the output of the holey VCSEL and a 2^7-1 pseudorandom bit sequence is used in the following BER measurement. Fig. 3(a) compares the measured BER at different data rates, when the TEC current is varied from 0 A to 1 A by 0.25 A step. A BER of $<10^{-11}$ is observed at 25 Gb/s at room temperature, as shown a dashed line in Fig. 3 (a). At 30, 35, and 40 Gb/s, the BER is changed from 4.3×10^{-6}, 1.0×10^{-3}, and 6.0×10^{-3} to 1×10^{-11}, 2.4×10^{-8}, and 6×10^{-4}, respectively, which is approximately linearly decreased with the TEC current. Fig.3 (b) compares the eye diagrams of 30, 35, and 40 Gb/s under TEC current at 0 A and 1 A. Under the cooling by TEC, the eyes are much clearer. This indicated that the TEC can be used to achieve a >30 Gb/s error free or a 40 Gb/s error under Forward Error Correction mask (10^{-3}) operation of holey VCSEL. The improved modulation performance can be attributed to the increased photon density and differential material gain at lower temperatures [6]. It should be note that the individual high-speed VCSEL in our current design occupies a wafer area of approximately 250×250 μm^2; with this small size of the VCSEL, a micro TEC can be used for VCSEL packaging in the future. Assuming reducing the TEC area to 250×250 μm^2, the power consumption of the TEC will only be on the order of ~0.1 mW, which is much smaller than the power consumption 36 mW of the VCSEL (13 m A and 2.8 V). In addition, appropriate packaging is needed to avoid vapor condensation, and thus the VCSEL can operate at an even lower TEC temperature. With these prospects, this integration approach can be very promising to achieve a low cost, low power, high data rate (> 40 Gb/s) VCSEL package.

In summary, a 25 Gb/s error-free operation of the directly modulated holey VCSEL is demonstrated at room temperature. By cooling the VCSEL with a TEC, the error-free modulation data rate can extended over 30 Gb/s. The integration of a micro TEC and a high-speed holey VCSEL will be pursed in the future, which will further reduce the power consumption of the VCSEL package.

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