Design and Analysis of a Compact UWB Pulse Generator With Programmable Pulse Shape

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***Abstract*—We present a programmable ultra-wideband (UWB) pulse generator designed and simulated in 90nm CMOS technology. The design receives an input square pulse and uses a pulse-combinatorial method to generate an output pulse composed of six individual impulses, each independently adjustable in both amplitude and delay. Additionally, the final pulse width can be adjusted. The design uses a 1.2V supply and is compact (core area ~0.1 mm^2). A digital memory block is used to retain the control bits that describe two different pulse shapes for purposes of demonstrating binary modulation schemes, including phase-shift keying, pulse-position modulation, or pulse-shape modulation at rates up to 2 Gbps. The design can produce pulses respecting the FCC-defined UWB indoor frequency mask, and consumes about 54 mW at the peak data rate, representing a pulse efficiency of 27 pJ/pulse.**

Keywords - CMOS; ultra-wideband (UWB); pulse combination method; pulse generation

I. INTRODUCTION

Impulse-radio ultra-wideband (IR-UWB) technology is expected to bring to fruition new opportunities for short-range wireless communication at very high data rates and low power levels for a variety of applications including wireless personal-area-networks (WPAN) and for sensing and high-resolution radar imaging. IR-UWB transmissions make use of short pulses with low power spectral density to ensure that the pulses exhibit minimal interference in a signal environment populated with carrier-based (narrowband) signals [1]. To this end, pulse generators designed for UWB communication are subject to several criteria: they should be low-cost; compact; energy-efficient; capable of forming pulses that conform to a particular frequency mask defined by a regulatory body such as the Federal Communications Commission (FCC) in the U.S.; compatible with popular UWB modulation formats like pulse-position modulation (PPM) and phase-shift keying (PSK); and ideally would feature some flexibility to respond to potentially changing constraints of the signal environment or channel.

Several possible chip-based implementations of UWB pulse generators have recently been proposed. Some rely on upconverting a baseband pulse using a mixer, which does not take full advantage of UWB's potential for power-efficient non-heterodyne architectures, and for which leakage of the local oscillator makes respecting the power spectral density requirements of UWB difficult. Other strategies have involved either adding discrete passive components or external filtering to shape the pulse [2], [3], requiring space-consuming inductors and tending to be inflexible. One attractive alternative to these practices is the so-called pulse-combination method (PCM) [4], [5] which is straightforward to implement in CMOS. PCM involves transforming the input rising/falling edge of a square-shaped input signal into a roughly triangular-shaped impulse, generating copies of this impulse by using multiple taps, then scaling each pulse by choosing tap coefficients (positive and negative), and recombining the impulses at small offset delays from each other to form the final UWB pulse to be passed to an antenna. Integrated implementations of PCM can use a distributed transversal filter [6] to perform the necessary pulse-delay function between taps – however this consumes a lot of chip real-estate due to the presence of inductive components in the unit cell delay line of each tap. A more compact approach involves using CMOS starved-inverters as delay elements [7], which is attractive also for their simplicity and easy voltage-controlled tunability.

The versatility of using PCM to generate an UWB pulse is evident in the multiple ways control signals that can be applied – previous demonstrations have illustrated either practical gain-control mechanisms to achieve widely tunable tap coefficients [6], or mechanisms for controlling the overall length of the output pulse [7]. In this paper, these ideas are combined in a single 90nm CMOS circuit, and integrated with an additional key functionality not present in previous CMOS-based PCM designs: the ability to fine-tune the delay offset of each individual impulse, adding a greater degree of flexibility in tuning output pulse shapes. We report the generation of several pulses of interest using this architecture that fit the FCC-defined spectral mask [8], and demonstrate power-efficient modulation of the pulse-shapes at rates of up to 2 Gbps (among the highest currently reported rates), which can be used for 2-PPM, binary PSK (BPSK), or even more exotic formats such as pulse-shape modulation (PSM) using orthogonal pulse shapes.

This paper is organized as follows: in section II, we describe the proposed PCM architecture for the UWB transmitter. In section III, we present simulation results to illustrate the pulses that can be generated and illustrate their performance with some simple binary modulation formats.

II. ARCHITECTURE

Our proposed architecture (Fig. 1) implements a compact six-tap PCM that provides several degrees of control for

shaping the final output pulse. In the first segment, an input square pulse is passed through three series and three shunt delay stages, each containing starved-inverters whose currents are controlled by analog control voltages. The series delay elements are controlled by a single common control voltage, the tuning of which has an accordion-like temporal stretching effect on the final output pulse, determining (along with the duration of the input pulse) the duration of the final UWB output. This is supplemented by the shunt delay stages (also starved-inverters), each of which features two independent control voltages that allow the fine-tuning of the individual sub-pulses – each control voltage controls independently the delay of a rising or falling edge, respectively. Only three shunts (taps) are necessary to control six sub-pulses; each rise and fall of the input signal is used to generates a sub-pulse oriented upwards or downwards. This is in contrast to previous works, in which a single rising or falling edge was the only impetus for the entire output pulse, requiring twice as many taps. An inverter is placed on even numbered taps to ensure that consecutive sub-pulses are inverted relative to each other (anticipating the alternating nature of the sub-pulses that comprise a traditional UWB pulse).

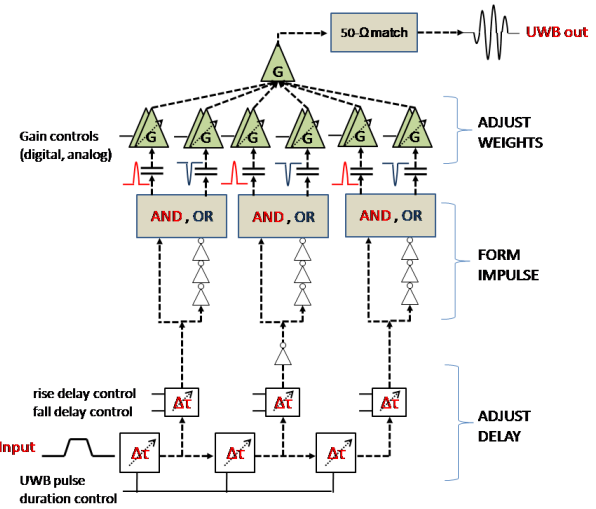

Figure 1. Schematic of the proposed architecture for UWB pulse generation.

The impulse-forming network follows the delay control block. It is composed of traditional 2-input CMOS logic cells operating on the input and a delayed, inverted copy of the input. Logical AND/OR functions are used to generate an upward pulse from a rising edge and a downward pulse from a falling edge, respectively. The delay between inputs is set to generate internal up- and down-impulses of 350 mV amplitude around a central bias point of 600 mV, half of the supply voltage.

The upwards- and downwards-oriented pulses are capacitively-coupled through a 250fF capacitor to a bank of parallel amplifiers that provide the weights to each pulse. Following the procedure to achieve a large dynamic range of gain established in [6], seven parallel single-ended common-source gain stages with on/off current-steering are assembled in three groups: four, two and one. Each of these three groups is collectively enabled by one bit of a 3-bit binary code, yielding one of $2^3 = 8$ possible discretely selected gain values for each pulse. The digital values describing a particular UWB pulse-shape can then be stored in memory as a sequence of 6 sub-pulses x 3 bits = 18 bits. The large dynamic range available with this technique is complemented by having an analog control voltage on the current of the solitary amplifier (the least-significant bit) to allow fine-tuning of the gain between discrete levels, either through direct tuning or a suitable digital-to-analog converter (DAC) where too many analog pads and control voltages would be cumbersome.

Each block of gain cells operates with a shared resistive load. The outputs are capacitively-coupled (250 fF) to a common node connected to an output stage consisting of two series common-source stages (for additional gain) and an emitter-follower at the output to buffer the signal to meet a 50-Ω load. A shunt capacitor is used at the load to approximate the effect of an output pad.

Several data modulation options are available with this architecture. First, we observed that attempts to directly modulate the gains by toggling the control-bits of a block of gain cells would inject unacceptable switching noise directly into the output signal between bits. We investigated the possibility of implementing each gain cell in a quasi-differential configuration, with different (static) gain settings in each branch, however, switching to select an output between these branches continued to generate unacceptable transients at the output. Instead, returning to single-ended gain-cells, the entire architecture was doubled, adding a second signal path, with the modulation toggling the path for the input square-wave trigger down one path for a given symbol, and the second for another. Although inefficient in terms of space and power, modulation with this strategy was free of unwanted transients (since it is performed before the digital delay block) and there is the added capability for each generated symbol to have entirely different delay values from the delay-setting circuit as well as different tap weights. The second path was given a 180-degree phase shift (by inverting the input signal), such that BPSK could be implemented simply by switching between paths with identical settings down each branch.

PPM can also be implemented in this architecture within a limited number of timeslots by choosing the same gain values and delays for each pulse while shifting which sub-pulses are present in the final output. For example, the design is capable of a simple PPM scheme with a three sub-pulse UWB signal (operating within our constraint of having only six sub-pulses). Shifting the output by three sub-pulses in the second branch represents a time-shift of approximately 150 ps for a minimum-width UWB pulse (approximately 380 ps), and it is clear that adding more taps would increase the flexibility and complexity of the symbols that could be transmitted by hopping timeslots.

III. Simulation Results

The proposed design was simulated in a CMOS 90nm process with a 1.2 V supply using the Cadence software suite. Settings for delay and gain control (analog and digital) were adjusted to yield the target pulses. Simulations were carried out at a high-level of detail and included parasitic elements. A 50-ohm load was assumed at the output pad. The simulated output is DC-coupled, although in practice it would be passed to an antenna with some frequency response that would filter the DC

offset, which is 176mV. The flexibility of the design makes *a priori* adjustment for the antenna's spectral response straightforward. We demonstrate in Fig. 2 a full-scale output with all six sub-pulses having maximum gain, and we show the tunable gain range of a single sub-pulse using only the digital control bits at each of the 8 possible settings. As mentioned, an analog control voltage on the least-significant control bit gives added flexibility to continuously tune between these discrete gain steps as in [6]. We also demonstrate in Fig. 3 the control of the temporal delay of a single sub-pulse within the output by tuning an analog control voltage (controlling the current in a current-starved inverter in the delay control block). It is noted that the neighboring pulse amplitude is slightly affected when the maximum delay is applied to the sub-pulse due to the coupling and summation of sub-pulses at a single common node, and it can be mitigated somewhat by using larger capacitances.

One commonly targeted capability for UWB pulse generators is to form a pulse compliant with the indoor frequency-mask for UWB communication proposed by the FCC [8]. Two examples of such pulses are illustrated in Figures 4 and 5 using the 4th-order and 5th-order derivatives of a Gaussian pulse, which we have normalized to 0V DC from our simulation by subtracting the output DC offset in MatLAB. Such Gaussian-derived pulses are in favor because their spectral properties are a fair fit with the full FCC-mask (contrasted to lower-order pulses) without having too much length to preclude a high data-rate (as higher-order pulses). Excellent agreement is demonstrated between the theoretical and simulated result. The frequency response of these pulses, found through the fast Fourier transform (FFT) in MatLAB, is presented in Fig. 6 (normalized to 0 dBm – actual ceiling would be at approximately -41.7dBm) and indicates the clearance of the FCC UWB spectral mask for these pulse shapes.

In Fig. 7, we demonstrate a simple BPSK pattern at 2 Gbps using the FCC-fitted pulse from Fig. 4 on both branches. In the figure, we show the input square-pulse stimulus, the modulating signal, and the circuit output.

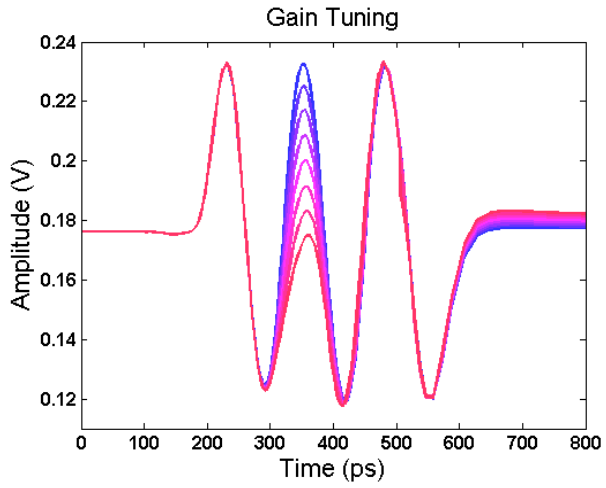

Figure 2. The full six-pulse UWB output with maximum gains applied. Tunability of an individual sub-pulse is demonstrated by enabling between 0 and 7 parallel amplifiers using a 3-bit input.

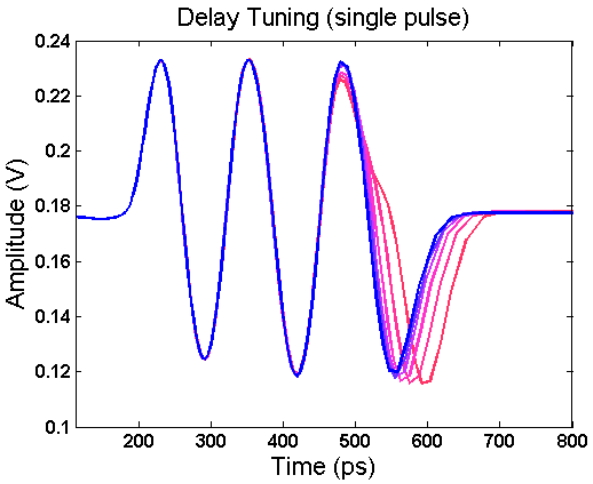

Figure 3. The full six-pulse output with maximum gains applied. Tunability of the delay of an individual sub-pulse is demonstrated by changing an analog control voltage from 900mV to 300mV in 100mV increments.

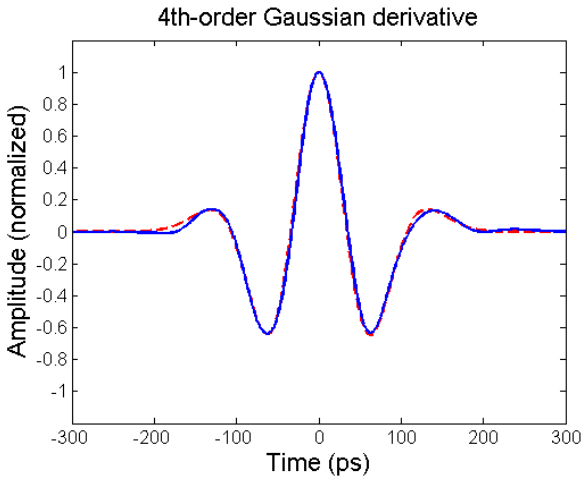

Figure 4. A 4th-order Gaussian derivative, theory (dashed) and simulation data from proposed design (solid).

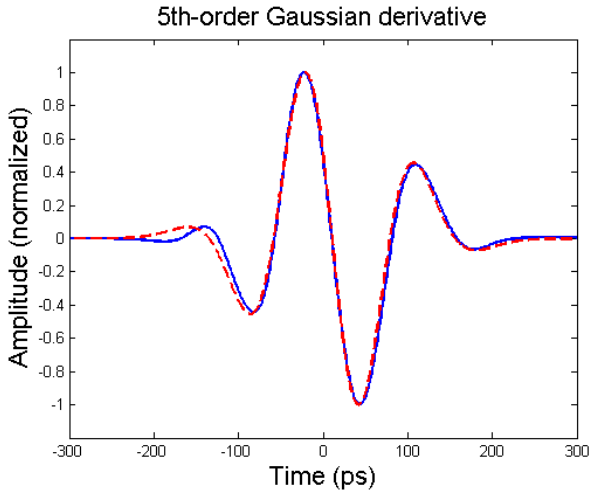

Figure 5. A 5th-order Gaussian derivative, from theory (dashed) and simulation data from proposed design (solid)

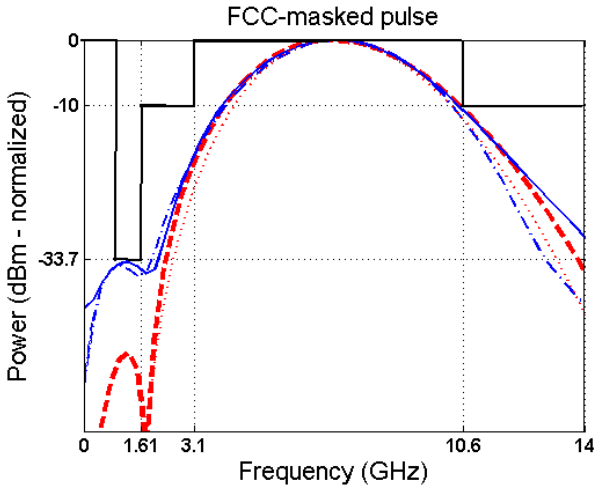

Figure 6. Frequency content of pulses from figures 4 and 5, both theoretical (4^{th}-order dash, 5^{th}-order dot) and from FFT of simulation (4^{th}-order solid, 5^{th}-order dash-dot)

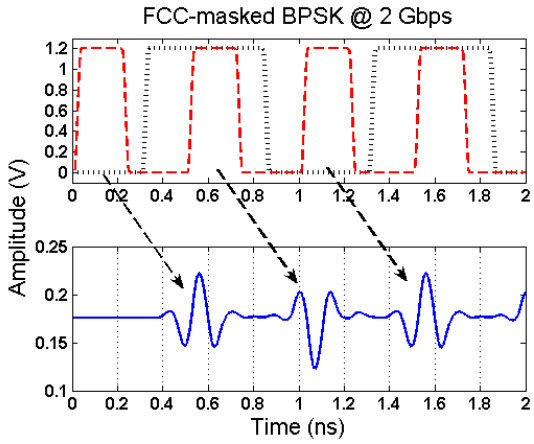

Figure 7. BPSK at 2Gbps. Top graph shows the input stimulus (dash) and data modulation signal (dot). Bottom graph shows UWB output pulses designed to fit the FCC-defined frequency mask.

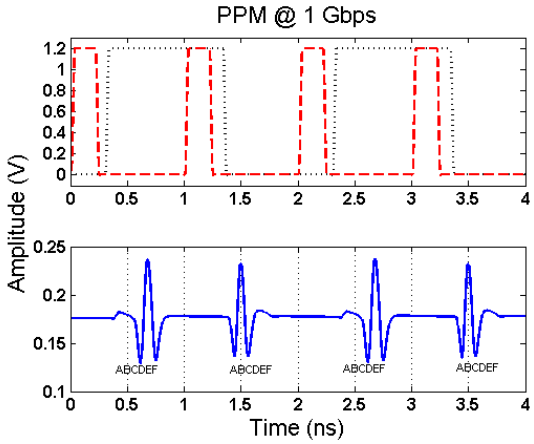

Figure 8. PPM at 1 Gbps by choosing sub-pulses; each of six sub-pulses is labeled A-F). Top graph shows the input stimulus (dash) and data modulation signal (dot). Bottom graph shows UWB output pulses using either the A-B-C or D-E-F sub-pulses.

This can be seen as a specific case of a more general capability of the circuit to perform binary pulse-shape modulation (PSM) between two different pulse shapes. In PSM, orthogonal pulses are typically sought (or at the very least, pulses which can be subject to orthonormal detection through design of a receiver template) [9]. The complexity and length of the pulses in an M-ary PSM scheme would determine the necessary number of taps and parallel channels in a PCM implementation.

As mentioned, the architecture is also capable of PPM, through two means. Working with all sub-pulses engaged, it is possible to choose different delay values for each signal path using the available controls in the delay block, and thereby assign a different total delay value to each brance. Alternatively, if a pulse does not use all available sub-pulses, the pulse can be shifted a number of slots over by representing it using different sub-pulses. An example of this with a 3-pulse UWB output (not FCC-compliant) being position-modulated at 1 Gbps is presented in Fig. 8.

The predicted power consumption of the circuit (not including a 38-bit digital memory block) at the maximum data rate of 2 Gbps is approximately 54 mW, indicating a pulse power efficiency of about 27 pJ/pulse for this system, which is superior to those in the works referenced in Table III of [10], and competitive with the most recent demonstrations [11], although the pulses of this simulated system have a relatively lower peak-to-peak voltage of about 120mV.

IV. Conclusion

We have proposed, designed and numerically demonstrated a highly flexible implementation of a pulse-combination method to shape UWB pulses in 90-nm CMOS technology with a small working core area (approximately 0.1 mm^2, mostly taken up by a bank of 250 fF capacitors). Data rates of up to 2 Gbps and several types of data modulation, including BPSK, PSM and PPM, are demonstrable with this configuration. Output pulses are 120mV (peak-to-peak) and chip power consumption is predicted to be approximately 54mW at a 2 Gbps modulation rate.

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References

[1] G. R. Aiello and G. D. Rogerson, "Ultra-wideband wireless systems," IEEE Microwave Mag., vol. 4, no. 2, pp. 36-47, June 2003.

[2] L. Smaïni et al., "Single-chip CMOS pulse generator for UWB systems," IEE J. Solid-State Circ., vol. 41, no. 7, pp. 1551-1561, July 2001.

[3] Z. N. Low, J. H. Cheong, C. I. Law, "Novel low cost higher order derivative Gaussian pulse generator circuit," IEEE Singapore Int. Conf. Commun. Syst. ICCS, pp. 30-34, Sept. 2004.

[4] H. Kim, D. Park and Y. Joo, "All-digital low-power CMOS pulse generator for UWB system," Electron. Lett., vol. 40, pp. 1534-1535, Nov. 2004.

[5] M. Demirkan and R. R. Spencer, "A low-sensitivity on-chip impulse radio pulse generation method," Proc. IEEE 38th Asilomar Conf. Signals, Syst. Comput., p. 1020, Nov. 2004.

[6] Y. Zhu, J. D. Zuegel, J. R. Marciante and H. Wu, "A 0.18 μm CMOS distributed transversal filter with binary-weighted gain cell design," Top. Meet. Solicon Monolithic Integr. Circ. RF Syst. (SiRF07), pp. 227-230, Jan 2007.

[7] H. Kim, Y. Joo, S. Jung, "A tunable CMOS UWB pulse generator," ICUWB: IEEE Int. Conf. Ultra-WideBand – Proc., pp. 109-112, Sep. 2006.

[8] Federal Communications Commission, Government Printing Office, Washington: "First report and order: Revision of part 15 of the commission's rules regarding ultra-wideband transmission systems," ET Docket 98-153, Apr. 2002.

[9] J. A. Ney da Silva and M. L. R. de Campos, "Spectrally efficient UWB pulse shaping with application in orthogonal PSM," IEEE Trans. Commun., vol. 55, no. 2, pp. 313-322, Feb. 2007.

[10] M. Demirkan and R. R. Spencer, "A pulse-based ultra-wideband transmitter in 90-nm CMOS for WPANs," IEEE J. Solid-State Circ., vol. 43, no. 12, pp. 2820-2828, Dec. 2008.

[11] V. V. Kulkarni, M. Muqsith, K. Niitsu, H. Ishikuro and T. Kuroda, "A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB Transmitter With Embedded On-Chip Antenna," J. Solid-State Circ., vol. 44, no. 2, pp. 394-403, Feb. 2009.