Experimental Demonstration of a Novel 5/10-Gb/s Burst-Mode Clock and Data Recovery Circuit for Gigabit PONs

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Abstract: A novel 5/10-Gb/s burst-mode receiver featuring instantaneous (0-bit) phase acquisition for any phase step (±2π) between packets in GPON is demonstrated. Our design is based on an oversampling local oscillator and a phase picking algorithm.

OCIS codes: (060.4250) Networks; (060.4510) Optical communications

1. Introduction

Gigabit-capable passive optical networks (GPONs) are an emerging multi-access network technology that provide a low-cost method of deploying fiber-to-the-home. Fig 1(a) shows an example of a GPON with our work in context. In the upstream direction, the network is point-to-multipoint: using time-division multiple access (TDMA), multiple optical network units (ONUs) transmit bursty data to the optical line terminal (OLT). Due to optical path differences, packets can vary in phase and amplitude. To deal with these variations, the OLT requires a burst-mode receiver (BMRx). The BMRx front-end is responsible for amplitude recovery (most recently demonstrated in [1]), whereas clock and data recovery (CDR) is performed with phase acquisition by a clock phase aligner (CPA). This paper focuses on the CPA aspect of the BMRx.

The most important characteristic of the CPA is its phase acquisition time which must be as short as possible. In [2], the authors proposed a CPA at 622 Mb/s by making use of an oversampling CDR operated at twice the bit rate and a phase picking algorithm. In this paper, we demonstrate a 5 Gb/s BMRx that achieves instantaneous (0-bit) phase acquisition for any phase step $|\Delta\varphi| \leq 2\pi$ rads, between consecutive packets, with packet loss ratio (PLR) $< 10^{-6}$ and bit-error rate (BER) $< 10^{-10}$. In addition, we achieve this in a much more cost-effective manner by employing a simple local oscillator (LO), and thus eliminating the need of complex and expensive CDR circuits based on phase-locked loops (PLLs).

2. Burst-mode receiver configuration

A block diagram of the BMRx is shown in Fig 1(b). An LO or a CDR can be used to either generate a clock signal, or recover the clock from the incoming bursty data, respectively. The CDR/LO is followed by a 1:16 deserializer from Maxim-IC (MAX3950). The lower rate parallel data is then brought onto a Virtex IV field programmable gate array (FPGA) from Xilinx for further processing. On the board, it is first necessary to further parallelize the data and clock to a lower frequency that will ensure proper synchronization and better stability of these signals before they can be sent to the CPA for automatic phase acquisition. Thus, an integrated double-data rate (DDR) 1:8 deserializer is implemented on the FPGA. Automatic detection of the payload is implemented on the FPGA through a framer and a comma detector that are responsible for detecting the beginning (delimiter) and the end (comma) of the packets, respectively.

The CPA makes use of a phase picking algorithm and an LO/CDR operated in 2× oversampling mode. The CPA is turned ON for the PLR measurements with phase acquisition for burst-mode reception ($\Delta\varphi \neq 0$ rad); otherwise it can be by-passed for continuous-mode reception ($\Delta\varphi = 0$ rad). The realigned data is then sent to a custom BER tester (BERT). Note that, while a conventional BERT can be used to make the BER measurements, PLR measurements on discontinuous bursty data are not supported.

The idea behind the CPA is based on a simple, fast, and effective algorithm. Since the data is sampled twice per bit, the odd samples and even samples [*O* and *E*, respectively, in Fig 1(b)], sampled on the alternate (odd and even) clock rising edges [see t_{odd} and t_{even} in Fig 1(d)] are identical. The odd samples are forwarded to path *O* and the even samples are forwarded to path *E*. The byte synchronizer is responsible for detecting the delimiter. It makes use of a payload detection algorithm to look for a preprogrammed delimiter. The two byte synchronizers attempt to detect the delimiter on either the odd and/or even samples of the data respectively. That is, regardless of the phase step between two consecutive packets (±2π rads), there will be at least one clock edge [either t_{odd} or t_{even} in Fig 1(d)] that will yield an accurate sample. The phase picker then uses feedback from the byte synchronizers to select the right path from the two possibilities.

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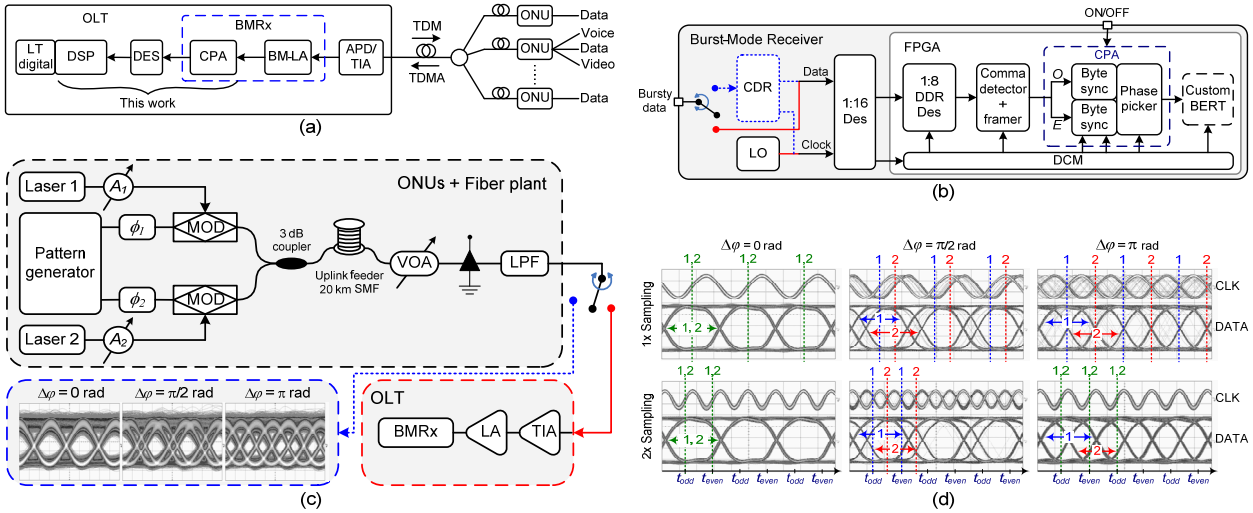

Fig 1. (a) Generic PON showing our work in context (APD: avalanche photodiode; TIA: transimpedance amplifier; BM-LA; burst-mode limiting amplifier; Des: deserializer; DSP: digital signal processing), (b) GPON OLT BMRx block diagram (DCM: digital clock manager), (c) GPON uplink experimental setup with typical bursty traffic, (d) Response to bursty traffic by sampling at bit rate and at twice the bit rate.

3. Experimental results and discussion

A block diagram of the GPON uplink experimental setup is shown in Fig 1(c). Bursty upstream PON traffic is generated by adjusting the phase, between alternating packets from two programmable ports of a pattern generator which are then used to drive their respective modulators (MOD). The amplitude of the packets is adjusted by employing variable optical attenuators (VOA) at the output of each laser. These packets are formed from guard bits, preamble bits, delimiter bits, $2^{15} - 1$ pseudorandom binary sequence payload bits, and comma bits. A silence period consisting of phase step $|\Delta\varphi| \leq 2\pi$ rads (with a 1-ps resolution) and m consecutive identical digits (CIDs), can be inserted between the packets. The upstream signals from the two ONUs are then coupled and sent over a 20-km uplink single-mode fiber (SMF). Prior to photodetection, a VOA serves to control the received power level. The output of the photodetector is then low-pass filtered (LPF) by a fourth-order Bessel-Thomson filter whose –3-dB cutoff frequency is 0.7 × bit rate. At the OLT, the bursty signal is then amplified by a TIA. The amplified signal with different voltage swings is then equalized by a limiting amplifier (LA) before being sent to the BMRx.

Fig 2(a) shows the BER and the PLR performance of the GPON uplink as a function of the received signal power. The receiver achieves a sensitivity of –18 dBm where it attains error-free operation: BER < 10^{-10} and PLR < 10^{-6}. In comparing the BER and PLR performance by sampling at twice the bit rate versus sampling at the bit rate, we observe a slight improvement in the case of the PLR metric. This is expected as discussed earlier. However, a power penalty of less than 1 dB must be paid at a BER = 10^{-10} due to faster electronics.

Next, we discuss the PLR performance as a function of the phase step between consecutive packets. Before presenting the results at 5 Gb/s, it is interesting to observe the effect of increasing PON data rates. This is because GPON standards for 2.5 Gb/s (upstream) and above, are currently categorized for further study [3]. Fig 2(b) shows the PLR performance of the GPON uplink for different preamble lengths at 1.25 Gb/s with only the CDR and CPA turned OFF. The reason for a bell-shaped curve centered at 400 ps is that this represents the half bit period corresponding to the worst-case phase step, $\Delta\varphi = \pi$ rads, and therefore the CDR is sampling exactly at the edge of the eye diagram [see Fig 1(d)]. Preamble bits ("1010…" pattern) can be inserted at the beginning of the packets to help the CDR settle down and acquire lock. However, the use of the preamble reduces effective throughput and increases delay. As the preamble length is increased, there is an improvement in the PLR. We observe error-free operation for any phase step after 28 preamble bits. By switching ON the burst-mode functionality of the receiver with the CPA as shown in Fig 2(c), we observe error-free operation for any phase step ($0 \leq \Delta\varphi \leq 2\pi$ rads) with *no* preamble bits, allowing for instantaneous phase acquisition. We also plot the phase step response of the receiver with only the CDR at 2.5 Gb/s. Again, as expected, the curve is centered at 200 ps as this is the half bit period corresponding to the worst-case phase step at 2.5 Gb/s.

By replacing the PLL-based CDR with the oversampling LO, we obtain error-free operation for any phase step with no preamble bits for data rates up to 5 Gb/s as shown in Fig 2(d). To our knowledge, this is the first time that a BMRx has been successfully implemented without CDR circuitry. This novel design is simpler and cheaper, without any reduction in performance. We note that a sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet [4]. However, by reducing the phase

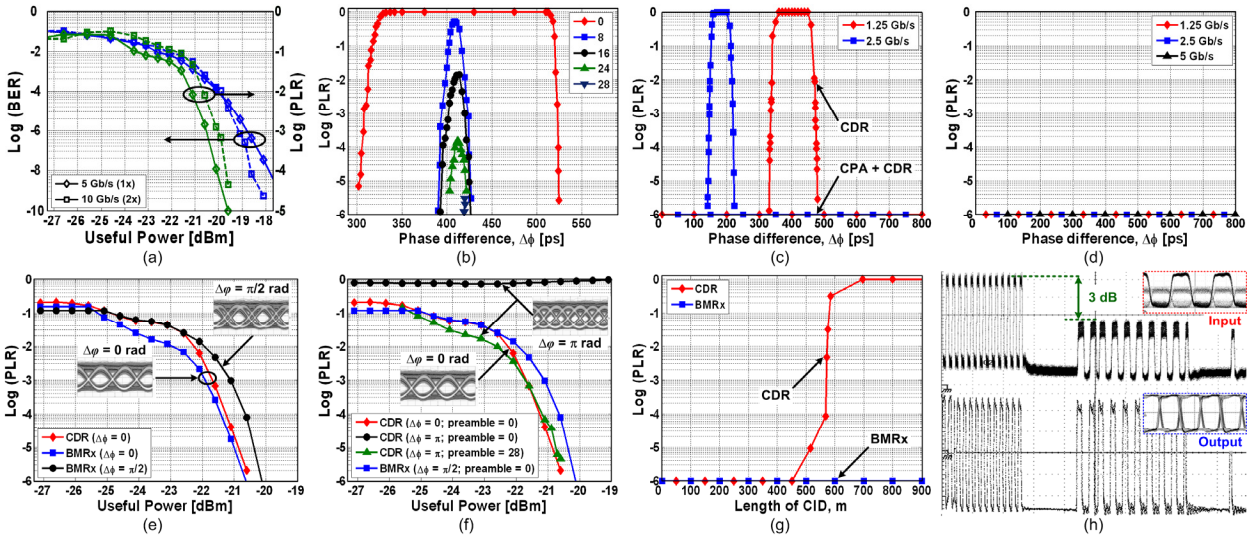

Fig 2. (a) PLR and BER vs. signal power. (b-d) PLR vs. phase step. (e) Burst-mode penalty. (f) Preamble length penalty. (g) PLR vs. CID immunity. (h) Measured input and output waveforms.

acquisition time, as demonstrated in this work, more bits are left for amplitude recovery, thus reducing the burst-mode sensitivity penalty. Alternatively, with the reduced number of bits, more bits can be used for the payload, thereby increasing the information rate.

To determine the burst-mode penalty of the receiver, we plot the PLR as a function of the received signal power in Fig 2(e). The PLR performance of the CDR sampling continuous data at the bit rate with no phase difference is compared to the PLR performance of the BMRx sampling bursty data with a worst-case phase difference, $\Delta\varphi = \pi/2$ rads. Both measurements are made for a 0-bit preamble. We observe a power penalty of less than 1 dB due to 2× oversampling and the phase picking algorithm. If there does exist a worst-case phase difference between the consecutive packets, the CDR will not be able to recover any packets, regardless of the signal power, resulting in a worst-case PLR ~ 1 as shown in Fig 2(f). However, if a 28-bit preamble is complied with, the PLR performance of the CDR is then comparable to the PLR performance obtained by the CDR with zero preamble bits and no phase difference. Hence, there is a tradeoff between the power penalty with the BMRx oversampling when $\Delta\varphi = 0$ rad [see BER plots in Fig 2(a)], and the number of preamble bits required without the BMRx when $\Delta\varphi \neq 0$ rad. Since phase steps in the GPON uplink are inevitable, the 1-dB power penalty may be a small price to pay than not receiving any packets. Fig 2(g) shows the CID immunity of the BMRx. The receiver can support more than 1000 CIDs with error-free operation, which is ~14× more than the minimum 72 CIDs specified in G.984.2.

The dynamic range of the receiver is measured to be 3 dB [see Fig 2(h)]. This relaxes the requirements of the output voltage swings/fluctuations from a front-end at high data rates. The dynamic range can easily be increased to 16 dB with a burst-mode amplitude recovery circuit as in [1]. Table I summarizes the performance of our receiver.

TABLE I. SUMMARY OF BMRX PERFORMANCE

	Bit rate (Gb/s)	Sensitivity (dBm)	Preamble (bits)	CIDs
This work	5	-18	0	> 1000
[1]	10	-19	1000	N/A
GPON [3]	1.25	-23	44	> 72

4. Conclusion

We have demonstrated a 5/10 Gb/s BMRx based on a 2× oversampling LO and a phase picking algorithm. We performed PLR measurements and quantified it as a function of phase steps between packets, signal power, and CID immunity. We also assessed the tradeoffs in power penalty and preamble length. The receiver achieves PLR < 10^{-6} and BER < 10^{-10} while featuring instantaneous (0-bit) phase acquisition for any phase step between packets, a sensitivity of –18 dBm, and supporting more than 1000 CIDs, with a power penalty of 1-dB. Our CDR-free BMRx greatly reduces the complexity of electronics, providing a cost effective solution for GPON receivers.

5. References

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