622/1244 Mb/s Burst-Mode CDR for GPONs

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***Abstract*— We present the design and test of a 622/1244 Mb/s burst-mode CDR for GPON OLT applications. Our design is based on a commercially available SONET CDR operated in 2× over sampling mode.**

I. Introduction

Passive optical networks (PONs) are an emerging access network technology that provides a low-cost method of deploying fiber-to-the-home. Fig. 1 shows an example of a PON network. In the upstream direction, the network is point-to-multipoint. Because upstream packets can vary in phase and amplitude due to optical path differences, the OLT requires a burst-mode receiver (BM-RX) and a burst-mode clock and data recovery circuit (BM-CDR). Within the OLT, the BM-RX is responsible for amplitude recovery, whereas the BM-CDR is responsible for phase recovery. This paper is about the design of a BM-CDR.

The most important characteristic of the BM-CDR is its phase acquisition time. Different approaches have been proposed to build CDRs with short phase acquisition times [1]-[8]. In this work, we use the over sampling (in time) approach and propose a novel phase picking algorithm. Our measurement results show that the BM-CDR meets the GPON physical media dependent layer specification defined in ITU-T Recommendation G.984.2 [9]. The CDR provides instantaneous phase acquisition (0 bit) for any phase step ($\pm 2\pi$ rad) and a BER < 10^{-10}.

II. Burst-Mode CDR

The main building blocks of the BM-CDR are a SONET CDR, a 1:16 deserializer, a byte synchronizer, and a phase picker (see Fig. 2). The BM-CDR supports three modes of operation: 1) conventional mode, 2) 2× over sampling mode, and 3) burst mode. The conventional mode of operation effectively makes the BM-CDR look like a conventional SONET CDR. The 2× over sampling mode is similar to the burst mode, the only difference being that the phase picker is turned off in the former case. The modes of operation are useful to measure the performance improvement between the SONET CDR and the BM-CDR.

The SONET CDR is from Analog Devices (part #ADN2819). The deserializer is from Maxim-IC (part #MAX3885). Its main function is to parallelize the data to reduce the bit rate. The parallel data and the divided clock are brought onto a Virtex II Pro FPGA from Xilinx for further processing. The phase picker and the byte synchronizer were implemented on the FPGA, alongside a burst bit error rate tester (BBERT) (see Fig. 2).

Our phase picking algorithm is both simple and fast. The idea behind it is to replicate the byte synchronizer twice. The two byte synchronizers attempt to detect the delimiter on the odd and even samples of the data, respectively. The phase picker uses feedback from the byte synchronizers to select the right path. Fig. 2 shows the phase picker right next to the two byte synchronizers to emphasize the fact that these three blocks work tightly together. For the conventional mode, the deserializer output (16 bits) is forwarded to path O (odd path); path E (even path) is disabled. This amounts to disabling the phase picker. For the 2× over sampling and burst modes, odd bits of the deserializer output (8 bits) are forwarded to path O and even bits are forwarded to path E.

III. Results and Discussion

Fig. 3 shows the burst-mode packet generator that we used to measure the phase acquisition time of the BM-CDR in its three modes of operation. The phase between two alternating packets can be adjusted on a 2 ps resolution and a ±2 ns range. Figs. 4 and 5 show plots of the packet lost ratio (PLR) vs. phase step for the BM-CDR operated in conventional mode (SONET CDR) and burst-mode, respectively. *In both figures, the preamble length was set to zero*. The plots of BER vs. phase step are not shown because the BER was < 10^{-10} for both modes of operation. This means that when a packet is not dropped (i.e. the delimiter is successfully detected in path O, path E, or both), then the payload is transmitted error free (PLR < 10^{-6}, BER < 10^{-10}). The BBERT uses the delimiter in order to trigger BBER measurements.

At 622.08 Mb/s, a 800 ps phase step corresponds to half a bit period (π rad). As expected, this corresponds to the worst-case phase step for the conventional mode (see Fig. 4). 40 preamble bits were necessary to obtain error free operation for any phase step. For the 2× over sampling mode (not shown), the worst-case phase step is 400 ps (or $\pi/2$ rad). As shown in Fig. 5, 2× over sampling, combined with our phase picking algorithm, turns a conventional CDR into a BM-CDR with instantaneous phase acquisition (no preamble bits).

The 622.08 Mb/s BM-CDR inherits the low jitter transfer bandwidth (1 MHz) and the low jitter peaking (0.1 dB) of the 1250 Mb/s CDR from which it is built. Likely, the 1244.16 Mb/s BM-CDR inherits the 2 MHz jitter transfer bandwidth and the 0.1 dB jitter peaking of the 2488.32 Mb/s SONET CDR from which it is built. Unlike the BM-CDRs in [1], [5], this BM-CDR does not trade off jitter characteristics for faster phase acquisition. Hence, in addition to PONs, this BM-CDR could find applications in burst/packet switched networks,

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which may require a cascade of BM-CDRs that each consumes some of the overall jitter budget of the system.

IV. Conclusion

In conclusion, we successfully implemented a 622.08/1244.16 Mb/s BM-CDR that meets G.984.2 specifications, provides instantaneous phase acquisition, and has good jitter characteristics. We verified the design at 622.08 Mb/s using a custom burst-mode test setup rated at 1 Gb/s (limited by the HP80000). The price to pay to obtain instantaneous phase acquisition is faster electronics. On the other hand, our solution exploits the design of components for long-haul networks. These components are typically a generation ahead of the components for multiaccess networks. For example, 10 Gb/s is currently mainstream for long-haul networks, whereas GPON supports a maximum data rate of 2.5 Gb/s. Assuming this holds true in the future, our solution will scale with the scaling of components for long-haul networks. Our solution also provides a cost effective alternative to the design of a custom ASIC.

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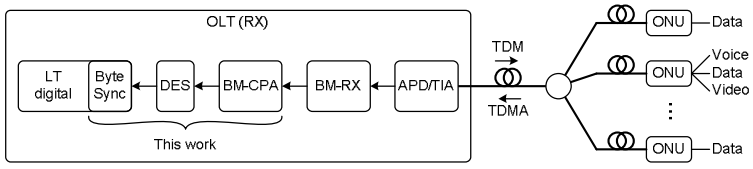

Fig. 1. Example of a PON network.

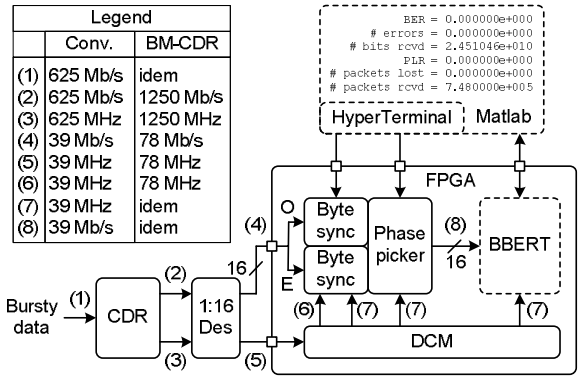

Fig. 2. BM-CDR.

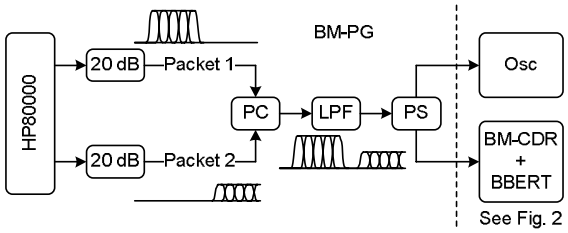

Fig. 3. Burst-mode packet generator.

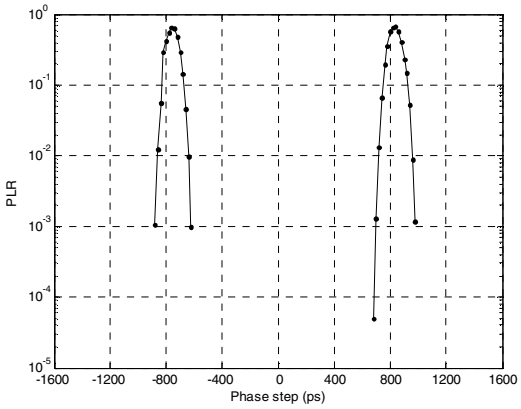

Fig. 4. PLR vs. phase step for a SONET CDR (622.08 Mb/s).

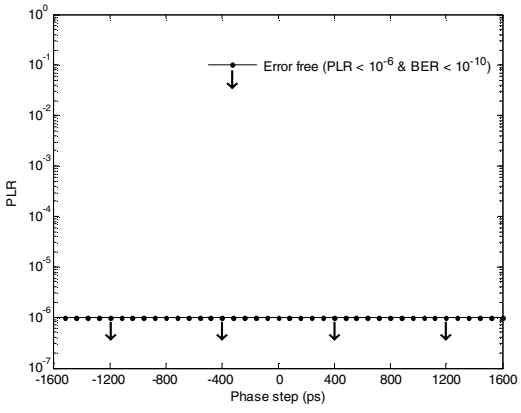

Fig. 5. PLR vs. phase step for the BM-CDR (622.08 Mb/s).