3.125Gbit/s Low Power Truly-Differential Parallel Optical Receiver Module in 0.13µm CMOS

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Abstract
High-speed, low-cost parallel optical receiver modules are needed in optically interconnected digital systems. High performance receiver designs become more challenging with the CMOS technology and supply voltage scaling down. In this work, we designed a 3.125Gbit/s, multi-channel, single 1.2V core supply optical receiver module in a 0.13µm triple-well CMOS process. The minimum power consumption including the post amplifier and the output buffer is 22.62mW per channel with a sensitivity of -16dBm. A method of using on-chip Pseudo Random Bit Sequence (PRBS) generator and dummy receiver channels to test the cross-talk performance was implemented. And also we present an accurate experimental method to characterize a photodiode array.

Keywords
Parallel optical receiver; transimpedance amplifier; 0.13µm CMOS; truly-differential; cross-talk, photodiode model.

1. INTRODUCTION
Very Short Reach (VSR) optics is a key enabler for future optically interconnected digital systems. These fiber links are replacing electronic counter parts because of their superior noise performance and bandwidth capabilities. At the receiver end, the preamplifiers with a common-gate (CG) input stage are frequently used for its low input impedance [1]-[3]. In order to compare the performances in a real testing environment, we have three different CG input-stage transimpedance amplifiers (TIA) designed and implemented on the same die.

In terms of optical receiver characteristics, sensitivity, noise, gain, bandwidth and power dissipation are the most important aspects. A successful design itself is to make reasonable trade-offs among these factors depending on the application.

Another important aspect in an arrayed receiver design is to achieve good channel isolation. Signals in one channel that coupled into other channels are simply just noises. For each type of the TIA, we built three channels side by side with a channel pitch of 250µm[1] to study the crosstalk performance. Substrate-coupling noise suppression techniques (e.g., deep-N-well and guard rings) are carefully implemented in the design. Empirical data are required as part of our long term goal of designing and fabricating a 12-channel optical receiver module.

[1] 250µm channel separation is determined by the bonding pitch of the available photodiode arrays.

2. ARCHITECTURE DESCRIPTION
Each receiver channel consists of a shunt-shunt feedback TIA, a Limiting Amplifier (LMA) and a Current-Mode-Logic (CML) output buffer to drive 50Ω load as shown in Figure 1. An Input Buffer (INB) is placed between the TIA and LMA to boost the signal amplitudes. To focus on the TIA performances only, the designs of the post amplifier and the output buffer are kept the same for all channels.

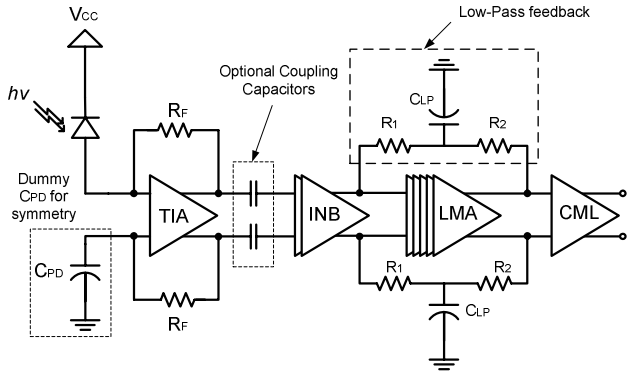

Figure 1. Optical receiver architecture

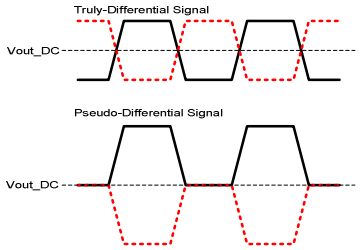

Figure 2. Pseudo-differential vs. truly-differential signals

An inherent problem of conventional differential TIA with a single-ended photodiode input is that the output swings are pseudo-differential as shown in Figure 2 [5]. This property makes the choice of the decision threshold difficult. We used two different designs to convert the pseudo-differential output into a truly-differential signal. The first design is to AC couple the TIA output to the post amplifier at a cost of introducing pattern dependent jitter (PDJ) into the system. The second design is to use a RC low-pass filter to extract the DC level of the TIA output and use it to bias the other branch of the differential topology (Figure 3(b) [5]). This method requires large resistor and capacitor val-

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ues to have a low enough corner frequency (less than tens of kilo hertz). We managed to realize this low-pass filter on-chip with high resistive polysilicon resistor (*266kΩ*) and dual-metal-insulator-metal (DMIM) capacitor (*12pF*), together they occupy 0.0067mm^2 chip area approximately.

2.1 Transimpedance Amplifier

Two of the three TIAs have a CG input stage followed by a differential-pair gain stage as shown in Figure 3 (a) (b). The feedback path is formed by a source-follower and a resistor for better noise performance. The source-follower provides level shifting purpose and also isolates the input and output of the amplifier. The *-3dB* bandwidth of the TIA is set by the pole on the input side due to the dominant role of the photodiode parasitic capacitance C_{PD}.

$$\omega_{-3dB} \approx \frac{A+1}{R_F C_{PD}} \qquad (1)$$

where A is the small signal gain of the amplifier, R_F is the feedback resistance.

The third design of TIA has a modified regulated cascode input stage (common gate feed-forward [4]), followed by a differential-pair with local feedback (Figure 3(c)). Theoretical work has been done thoroughly in [4]. This modified design is more suitable for low power and low supply voltage applications.

2.2 Limiting Amplifier

The limiting amplifier serves two functionalities: the first is to amplify the preamplifier output to digital level; the second is to limit the output amplitude so that it is independent of the input levels over the entire receiver dynamic range.

Usually the bandwidth of the limiting amplifier needs to be close to the data rate for two reasons. (i) When two system blocks with the same bandwidth cascading, the overall bandwidth is much narrower. (ii) But if the bandwidth is too high, it may result in excessive input referred noise increase in deep-submicron design due to the degrading of the transimpedance gain of the preamplifier [5].

The gain cell shown in Figure 4 is a simple differential pair which has high enough bandwidth in this application, so no other bandwidth extension techniques are used. The bandwidth is given by (2) when five gain cells are cascaded.

$$\omega_{-3dB} = \omega_0 \sqrt{\sqrt[5]{2}-1} = 0.35\omega_0 \approx 3.125GHz \qquad (2)$$

where ω_0 is the bandwidth of each gain cell.

In order to maintain the optimum biasing of the gain cell string, a first-order low-pass feedback loop [6] is used as shown in Figure 1. The resistor and capacitor used in this design is *266kΩ* and *12.5pF* respectively, which gives a low corner frequency of *48kHz*. That is low enough not to incur significant Inter-Symbol Interference (ISI). The resistors and capacitors are similar to those used in Figure 3 (b) for the low-pass filter.

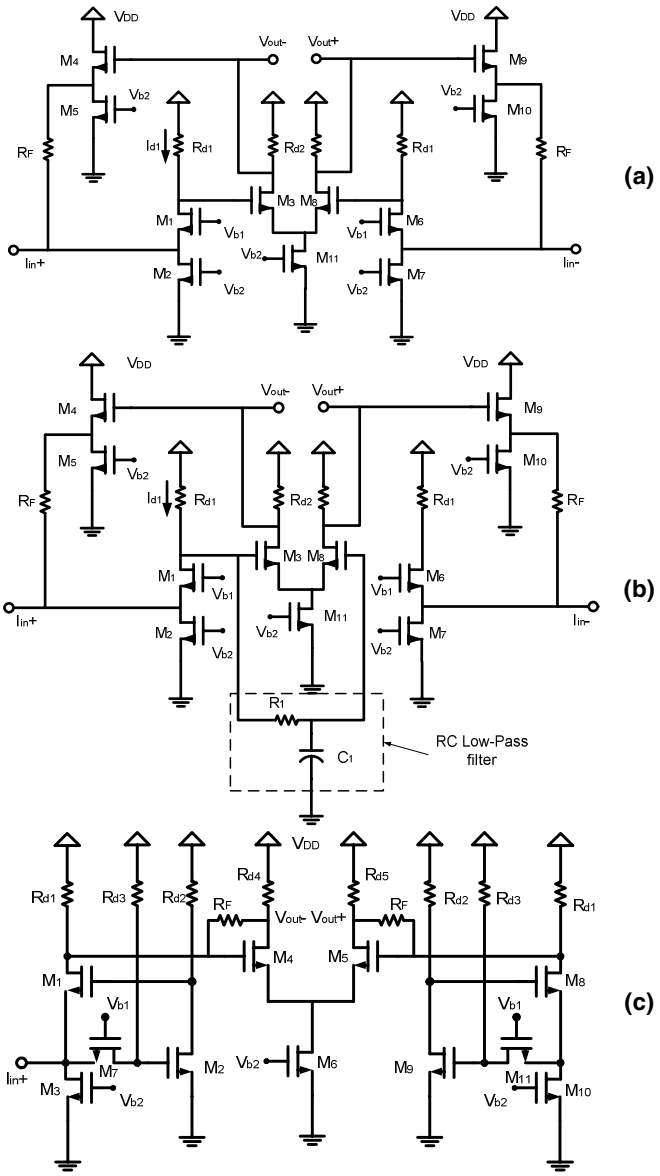


Figure 3. (a),(b) CG input stage TIA (c) CG feedforward input stage TIA

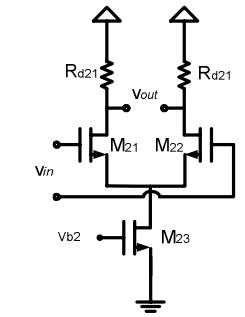


Figure 4. LMA gain cell

2.3 CML Output Buffer

A 3-stage tapered CML output buffer is used to drive 50Ω load as shown in Figure 5 [7]. The design parameters are shown in Table 1. The CML buffer can deliver a 300mV peak-to-peak differential output with moderate power dissipation.

Table 1. Design parameters of the CML output buffer

	Stage #1	*Stage #2*	*Stage #3*
I_{ss}	*888.8μA*	*2.67mA*	*8mA*
M_{ss}	*30um/0.36um*	*88um/0.36um*	*265um/0.36um*
M_n	*11um/0.12um*	*33um/0.12um*	*100um/0.12um*
R_{cml}	*450Ω*	*150Ω*	*50Ω*

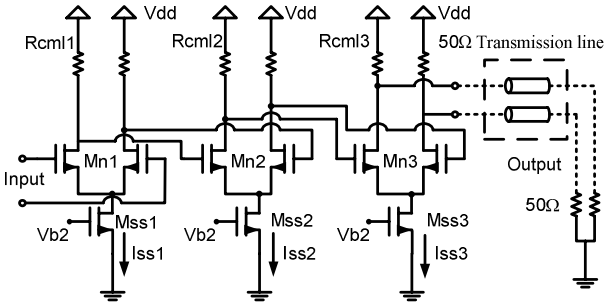


Figure 5. CML output buffer

3. CROSSTALK MEASUREMENT

To measure the crosstalk performance in the arrayed design, we have three channels for each type of TIA built side by side with a channel separation of 250μm which corresponds to the available photodiode array bonding pitch. Only the center channel is to be tested under the disturbance from the other two channels on the side, which are driven by an on-chip PRBS generator. This method is similar to what was used in [8]. The difference is the signal phase and amplitude of the interference channels are independent of the channel under testing in our design, which is more close to the working conditions in reality.

The reason for choosing three channels is that each receiver channel suffers crosstalk from their neighboring channels through the substrate. However, most of the crosstalk noises are contributed by its nearest neighbor. Hence the 3-channel arrangement will be adequate to study the crosstalk performance.

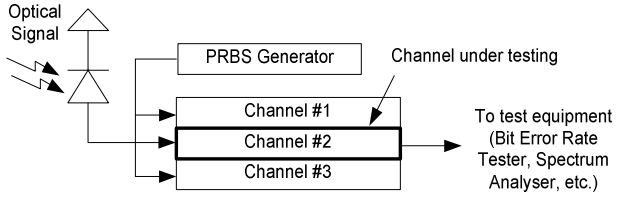


Figure 6. Cross-talk measurement diagram

4. PHOTODIODE MODELING

The photodiode (PD) parasitic capacitance is one of the dominant parameters that affect the TIA *-3dB* bandwidth. But this capacitance cannot be measured directly. So we constructed a PD model in *Agilent ADS* and built a setup to measure the S_{11} parameter with *Agilent Lightwave Component Analyzer 8703B*. The PD model and the test setup are illustrated in Figure 7, where $R_{BP1,2}$ and $C_{BP1,2}$ are the bond-pad series resistances and parasitic capacitances respectively; R_{SH} is the shunt resistance and C_{PD} is the PD parasitic capacitance. The bond-wire is represented by a single inductor in this model, L_{BW}. The C_{BP2}, R_{BP2} and L_{BW} are scaled by 2 due to 2 pads are used in the setup for the ground connections (Figure 7 (a)).

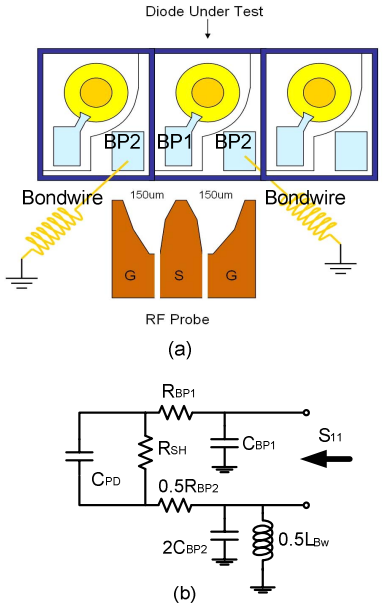


Figure 7. (a) S_{11} parameter test setup; (b) PD model used to determine all the parasitics.

The measured S_{11} curves of 3 photodiodes on a 1×12 PD array and the fitted curve are shown in Figure 8. This model was also verified in *Cadence Analog Environment* using *Spectre* simulator. Both simulation results from *ADS* and *Spectre* match the measured curves very well.

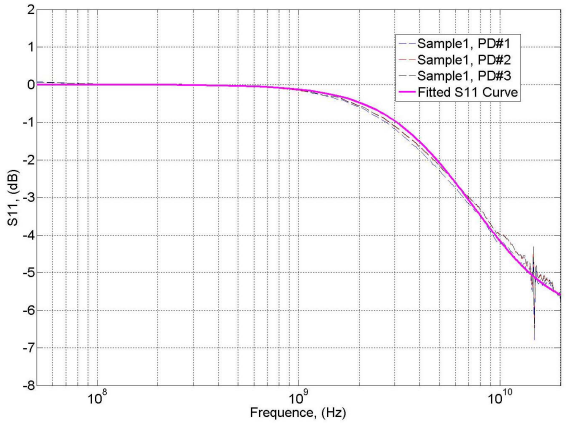


Figure 8. Measured S_{11} curves and the simulation result

The PD geometry features were measured with an interferometer profiler developed in our group which was used for MEMS experiments. 3D images are shown in Figure 9. The dark current was measured by *Hewlett-Packard 4145B*

Semiconductor Parameter Analyzer. The photodiode characteristics are summarized in Table 2.

Table 2. Measured photodiode parameters

C_{PD}	*Diode parasitic cap.*	*393.8fF*
C_{BP1}	*Anode bondpad parasitic cap.*	*61.76fF*
C_{BP2}	*Cathode bondpad parasitic cap.*	*181.04fF*
R_{BP1}	*Anode bondpad resistance*	*14.5Ω*
R_{BP2}	*Cathode bondpad resistance*	*9.7Ω*
R_{SH}	*Shunt resistance*	*518.8MΩ*
L_{BW}	*Bond-wire inductance*	*2.58nH*
I_d,	*Dark current*	*0.2~0.3nA*
Z_{PD}	*Bonding pitch*	*250μm*
D	*Active region diameter*	*~75μm*
A_{BP}	*Bondpad size*	*52×82μm²*

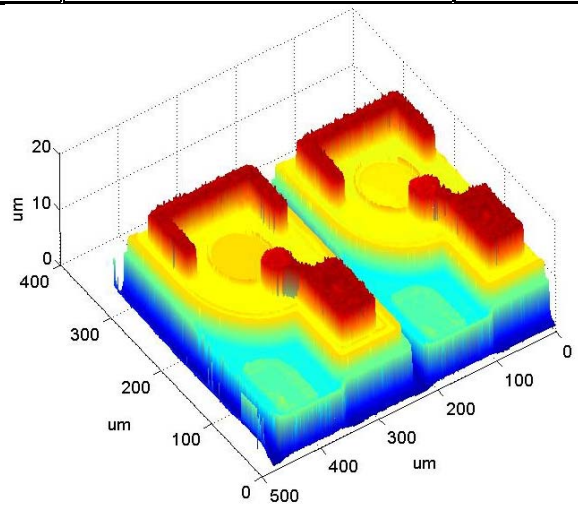


Figure 9. 3-D PD array image; two photodiodes are shown;

5. SIMULATED PERFORMANCE

The TIA designs are simulated with *Spectre* in the *Cadence Analog Environment*. TIA Performances are summarized in Table 3. All of the three TIAs are suitable for 3.125Gbit/s applications both in bandwidth and input referred noise levels. The differential transimpedance gains are all greater than *56dBΩ*. The lowest channel power consumption is 22.62mW including the LA and CML buffer.

Table 3. Simulated TIA performances

	CGAC	*CGDC*	*CGFW*
-3dB Bandwidth, GHz	*2.6GHz*	*2.1GHz*	*2.0GHz*
Input Referred Noise	*31pA/√Hz*	*23pA/√Hz*	*25pA/√Hz*
Transimpedance gain (differential)	*56.1dBΩ*	*57.3dBΩ*	*59.2dBΩ*
Quiescent Power Dissipation	*2.5mW*	*2.5mW*	*3.9mW*

The TIA and CML buffer output eye diagrams are simulated with PRBS signal inputs (bit sequence length 2^{15}-1). As shown in Table 4, the CML buffers provide constant 300mV differential peak-to-peak outputs over 50Ω load for *12.5μA* and *200μA* photo current. Assuming a photodiode conversion efficiency of *0.5A/W*, *12.5μA* and *200μA* photon current correspond to *-16dBm* and *-3.98dBm* optical power. The input photon current could be higher than *200μA*.

Of all the three TIAs, the CGDC type has the lowest input referred noise. Further more, it has less jitter compared to CGAC and CGFW types as can be seen from Table 4. The excessive jitter is introduced by the AC coupling capacitors used to convert the pseudo-differential signal to a truly-differential signal. It can be lowered by increasing the capacitance with sacrifice of the bandwidth or an increase of noise level.

6. LAYOUT

The chip is designed in IBM cmrf8sf-DM 0.13μm CMOS process and it is currently undergoing fabrication. The design is pad-limited which has a total area of 4mm^2 with a core of 1.2mm^2.

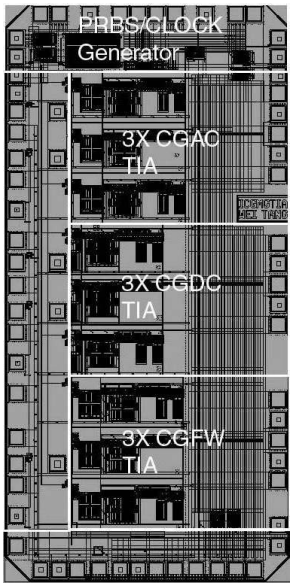


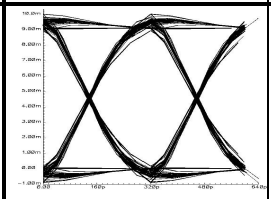
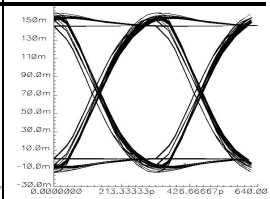
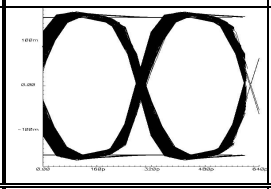
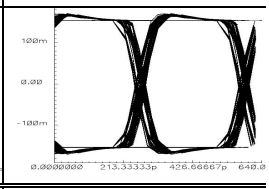
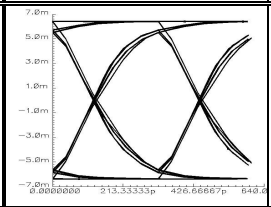
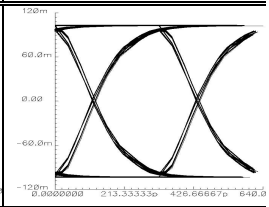
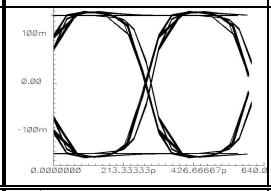
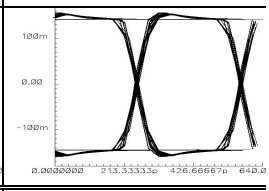
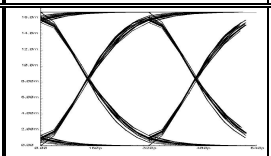
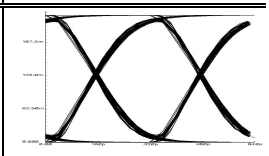
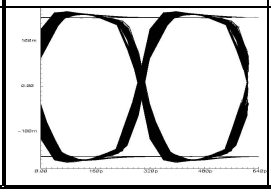
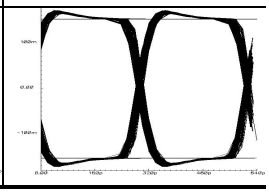
Figure 10. Chip layout view

To protect the sensitive analog circuitry from the noisy digital parts, all the NMOS transistors are put in deep-N-wells to suppress noises coupled via the substrate. Double P+ guard rings are used to surround each building block and every channel. ESD protections are used on the biasing pads only, because those pads are directly connected to the transistor gates.

7. CONCLUSION

We designed a 3.125Gbit/s parallel optical receiver module in 0.13μm CMOS that is suitable for VSR optical interconnects with a single 1.2V power supply. Of the three different TIAs implemented, the common gate DC coupled design has the best overall performance. All of the three designs can deliver a 300mV constant output signal to 50Ω load. Simulated performances will be verified after the chip shipped back from the foundry.

Table 4. Simulated output eye-diagrams with 2^{15}-1 PRBS inputs

Outputs		Photon Current 12.5μA	Photon Current 200μA
CGAC	TIA		
	CML		
CGDC	TIA		
	CML		
CGFW	TIA		
	CML		

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