A Broadband PLL solution for Burst-mode Clock and Data recovery in All-Optical networks

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Abstract: Fast phase-locking PLLs are proposed as a new solution for recovery of burst-mode data. Modeling and circuit implementation have demonstrated phase-lock times on the order of tens of bits for data recovery at OC-48 rates.

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1. Introduction

Demand for broadband access and services is exceeding the potential of modern electronics. All-optical networks have been proposed as a solution to enable services such as IP telephony and video on demand in metro and access areas [1]. All-optical networks are characterized by a point-to-multipoint topology supported by an all-optical core which is nearly absent of electronics. However, deployment of All-optical networks will require increased functionality in the electronics which will remain at network edges. In particular, clock and data recovery (CDR) electronics in optical receivers must be adapted to deal with burst-mode traffic rather than continuous-mode traffic seen in point-to-point networks. This presents a significantly different problem from conventional CDRs. Data bursts originate from various sources, each arriving at the receiver with a phase which can potentially change by $\pm\pi$ Rads. New CDR design is required to adapt to large steps in phase upon each new burst to maintain BER integrity. This phase recovery process must be completed on the order of ns if All-optical networks are to be viable [2].

2. The Broadband PLL solution

Most modern CDRs are based on Phase-Locked Loops (PLL) which have been designed to reflect the requirements of continuous-mode networks such as SONET. Specifically, the phase of incoming data is assumed to be constant with minimal drift and data is received as a continuous-wave without dead zones of non-transmission. These conditions allow for a solution based on a narrowband PLL, which has a small jitter bandwidth and is able to produce a clock which is highly resistant to phase variations. It therefore suffers from minimal jitter during retiming of data even when low-frequency components are present. This allows for high jitter-suppression qualities and a good BER. However, if recovering burst-traffic, the invariable nature of the narrowband PLL would imply very slow clock phase acquisition to steps in data phase. Testing of a commercially available OC-48 CDR in burst-mode has yielded phase lock-times on the order of 1400 bits, or μs at gigabit rates [3].

This work proposes broadband PLLs as a solution to the burst-mode clock and data recovery problem. The solution involves modification of the continuous-mode CDR architecture to reflect the requirements of burst-mode. This is accomplished by remodeling the traditional clock and data recovery PLL to increase loop bandwidth, which increases the internal gain of the loop. This creates a broadband PLL which would respond to phase-steps with a high-gain feedback response to re-acquire phase lock for optimal retiming of data. Such a loop can potentially recover clock phase to each new data burst at times on the order of tens of bits, or ns at gigabit rates.

This high-gain capability is made at the expense of jitter-suppression abilities. Increasing loop bandwidth (and jitter bandwidth) inherently allows more jitter to propagate from incoming data through to the recovered clock. Therefore, as the broadband PLL is unable to distinguish a true phase step from cycle-to-cycle data jitter, more jitter is allowed to propagate than in a narrowband CDR. Therefore, accurate modeling must be performed to set loop parameters as an acceptable tradeoff between jitter-rejection and lock-time acquisition. Also, broadband PLLs are prone to more clock phase drift when receiving low transition-density data. This makes high-density line coding necessary, such as 4B5B. Therefore the

tradeoffs of this solution are lower jitter rejection capabilities and a strong requirement for line coding. However, as All-optical networks are projected for metro and access deployment the jitter requirements would be less stringent than in long-haul and these tradeoffs may be acceptable.

3. Design Approach and Implementation

The circuit chosen for modification is a half-rate Charge-pump Phase-locked CDR intended for SONET which has previously been demonstrated to recover data in continuous-mode at 10Gb/s [4] (Figure 1).

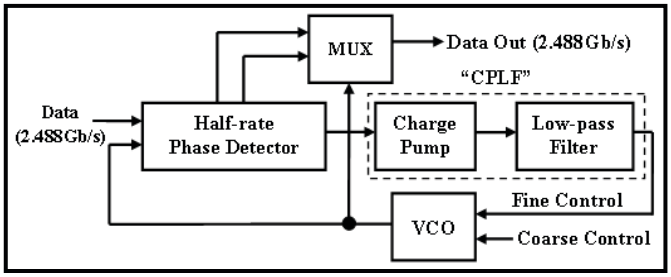

Figure 1: Half-rate Charge-pump Phase-locked CDR architecture

Adapting the narrowband architecture to yield robust broadband operation presented significant challenges. Firstly, stability is an issue in feedback loops if internal gain/bandwidth is made too high. Furthermore, traditional PLL models used to assess stability assume narrowband, allowing for time-invariant approximations of the system and continuous-time modeling. Additionally, small phase errors are assumed to allow linear approximations of loop behavior. Neither of these assumptions apply in the burst case.

To assess stability in broadband implementation the circuit parameters were related to 2nd-order control theory to determine loop gain/bandwidth, *K'*. A previous Z-domain analysis of Charge-pump PLLs was then used to determine a range of circuit parameters which would yield a stable system. The analysis does not assume narrowband and states that stability is assured if the following limit on loop gain is respected (ω_i is the frequency of the incoming signal and τ_2 is the time constant of the loop filter) [5]:

$$K' < \left[\frac{\pi}{\omega_i \tau_2} \bullet \left(1 + \frac{\pi}{\omega_i \tau_2} \right) \right]^{-1} \quad (1)$$

Another previous work has presented a time-domain model of 2nd-order Charge-pump PLLs which assumes neither narrowband nor small phase errors [6]. This model was used to assess broadband loop responses to phase steps over the range [0, ±π/2] Rads., encompassing all phase step possibilities in a half-rate CDR. Using this model a set of circuit parameters was derived to yield a broadband system which would respond to phase steps within nanoseconds. Linear gains and parameters were derived for the phase detector (K_{PD}=50mV/Rad), charge pump (K_{CP}=400μA/V), low-pass filter (R=5kΩ, C=2.5pF), and VCO (K_{VCO}=2GHz/V). Corresponding predictions from the time-domain model are shown in Figure 2. The CDR implemented with these parameters is shown in Figure 3. The chip is 1mmx1mm and consumes ~50mW.

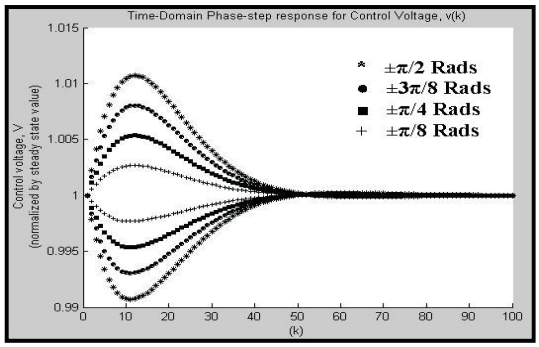

Figure 2: PLL feedback control signal responses to input phase steps: ±π/8, ±π/4, ±3π/8, and ±π/2 Rads.

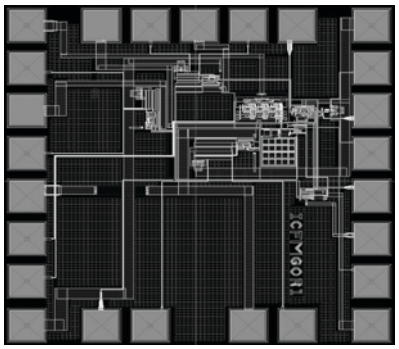

Figure 3: Broadband, Phase-locked, half-rate CDR implemented in CMOS 0.18

With these parameters the model predicts phase lock within 56 bits to steps of ±π/2 Rads., or 22.6ns at 2.488Gb/s. However, implementation of the phase detector did not meet target gain. Modeling with the actual

gain yielded a lock time prediction of 98 bits for ±π/2 Rads. Cadence simulations confirm a stable system and lock within 98 bits at 2.488GB/s. Jitter bandwidth and jitter peaking in the circuit may be calculated as follows:

$$\omega_{-3dB} = R \bullet K_{VCO} \bullet K_{PD} \bullet K_{CP} \quad (2)$$

$$JitterPeaking = 1 + (\omega_{-3dB} \bullet R \bullet C)^{-1} \quad (3)$$

The bandwidth and peaking of the original circuit are calculated to be 15MHz and 1.48dB, respectively, while our work yields a 100MHz bandwidth and 1.11dB peaking. These results confirm a wider bandwidth has been achieved, producing lower jitter suppression. However, lower jitter peaking is also exhibited.

4. Experimental results

At the time of this writing only preliminary continuous-mode testing had been performed. Preliminary results confirm clock recovery from high transition density data having no more than 4 consecutive identical bits at 2.488Gb/s. The clock spectrum shows peaking of -20dBm at 1.244GHz, a noise floor of -60dBm, and -3dB bandwidth of 400KHz, producing a Q-factor of 3.11×10^3. The frequency capture range is ±500KHz and the tracking range is ±10MHz. However, this performance degrades as transition density is lowered. Packaging issues at the time of this writing prevented data to be recovered from the chip at the target 2.488Gb/s rate. However, testing with a repeating "1010" pattern at 1.244Gb/s has yielded successful data recovery and a stable clock (Figure 4). Testing with a 2^7-1 PRBS sequence still yields recovered clock and data, however the clock is jittered (Figure 5). The recovered pattern and clock amplitudes are 120mV and 35mV peak-to-peak.

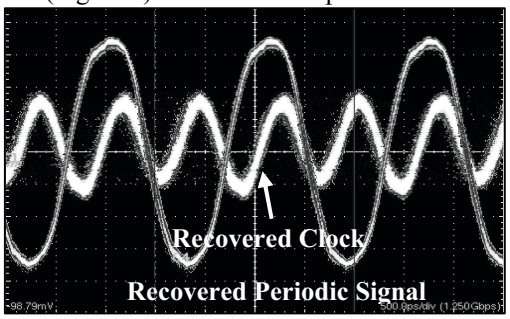

Figure 4: Recovered clock and pattern from alternating sequence at 1.244Gb/s. Clock is jittered.

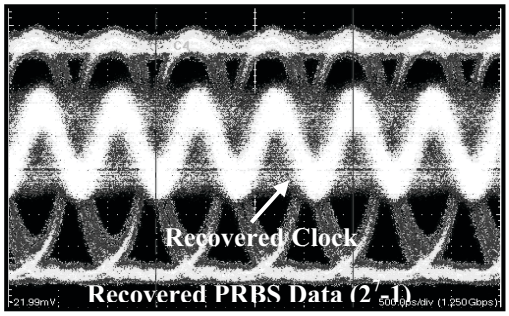

Figure 5: Recovered clock and data from a PRBS data sequence of 2^7-1 at 1.244Gb/s. Clock is stable.

While clock phase recovery time has not yet been determined these preliminary results confirm clock recovery and a stable system. New packaging is being prepared in order to recover data at the target rate and determine BER performance, as well as clock recovery time to burst data.

5. Conclusion

By modifying PLL parameters, Phase-locked CDRs may be adapted to recover burst-mode data within ns at gigabit rates at the expense of jitter and line coding, allowing for viable All-optical networks.

6. References

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