Performance of a multi-user OCDMA system demonstrator with full clock and data recovery

Julien Faucher, Rhys Adams, Lawrence R. Chen, and David V. Plant

Photonic Systems Group, Department of Electrical and Computer Engineering, McGill University 3480 University Street, Montréal, Québec, Canada, H3A 2A7 Tel: +1 514 398 2531, Fax: +1 514 398 5208, E-mail: julienf@photonics.ece.mcgill.ca

Abstract: We investigate the performance of a multi-user OCDMA system demonstrator with full CDR using a novel OCDMA receiver. We achieve sensitivities (BER $< 10^{-10}$, 2²⁰-1 PRBS) of -19.1, -16.3, and -9.2 dBm for 1-3 users. ©2005 Optical Society of America OCIS codes: (060.2330) fiber optics communication, (060.4510) optical communications

1. Introduction

Optical code-division-multiple-access (OCDMA) is a promising technology for use in optical access networks carrying bursty and asynchronous traffic [1]. 2D wavelength-time (λ -*t*) OCDMA has been explored as a means to provide greater flexibility in code design and increase system performance [2]. To date, most or all OCDMA technology demonstrators have relied on the availability of a global clock in system implementation and testing, especially for performing bit-error-rate (BER) measurements [3-5], which is not representative of a real functional access network. For OCDMA to be a competitive alternative to conventional multiple access schemes, such as TDMA and WDMA, full clock and data recovery (CDR) at the receiver end must be demonstrated. In this paper, we analyze the performance of a multi-user OCDMA system demonstrator with full CDR. The OCDMA receiver allows digital logic circuits to process OCDMA data in the same way as if TDMA or WDMA had been used in the transport network. These results show the viability of OCDMA as a transport technology for access networks.

2. OCDMA System Demonstrator and OCDMA receiver

The OCDMA system demonstrator is based on the 2D wavelength-time (λ -*t*) depth first search codes (DFSCs) described in [6]. While many different 2D λ -*t* code families exist, we have focused on DFSCs since they possess the following key advantages: (1) the codes can be designed using fewer time chips and thus are able to support higher data rates and (2) since for a given code dimension a greater number of codes can be generated, they can fully exploit the gain provided by forward error correction (FEC) to allow for a large number of simultaneous users operating with good BER performance [6].

In our system demonstrator, we use codes having 8 wavelengths (1547.6 nm - 1553.2 nm with 100 GHz channel spacing), 8 time chips, and a weight of 4, resulting in 31 possible codes. Of the 31 possible codes generated by the DFS algorithm, we use the 3 codes illustrated in Fig. 1. The 2 interferers (Enc 2 and 3) have been chosen such that each has 2 wavelengths in common with the desired user (Enc 1) thereby making the task of identifying the auto-correlation peak more difficult (this represents a worst-case scenario among the 31 codes generated by the DFS algorithm). The data rate is 155.52 Mb/s (OC-3) and the chip rate is 1.244 Gb/s (OC-24). A block diagram of the set-up is shown in Fig. 1.



Fig. 1. Block diagram of OCDMA system demonstrator and receiver

A "1" data bit is represented by a broadband pulse (modulated ASE from a broadband source) having a duration equal to the chip time; no power is transmitted for a "0" bit. The data bits are first split into three paths containing decorrelating fiber (to emulate different data patterns from the different users) and then optically encoded by three encoders before being recombined and propagated through fiber. The decoder performs matched filtering before detection. The encoders and decoder are constructed using commercially available wavelength de-/multiplexers, power splitters/combiners, and the time delays are obtained by splicing appropriate lengths of fiber. Each delay line is carefully measured and has less than \pm 5% of a time chip of error in order to minimize the effects of encoder/decoder mismatch. We ensure that all encoded signals are launched with approximately the same power. Unlike other OCDMA system demonstrations [3-5], we do not use a global clock at the receiving end to perform BER measurements. Instead, we recover the clock directly from the data using an OCDMA receiver. The target BER is 10⁻¹⁰ using a PRBS length of 2²⁰-1 for each user.

The OCDMA receiver is made of five building blocks (see Fig. 1): a photoreceiver (O/E), a quantizer (Q), a CDR for SONET applications, a 1:16 deserializer (Des), and a controller (Ctrl). The quantizer applies a threshold on the incoming data in order to filter out multi-access interference (MAI) from the two interferencs.

The CDR recovers the clock at twice the chip rate, or OC-48, to accommodate the 1:16 deserializer (2.48832 Gbps/16 = 155.52 Mbps). Clock recovery at OC-24 would also work provided a 1:8 deserializer is available. The advantage of two times over sampling is that it gives the falling edge of the recovered clock (the decision circuit in the CDR is negative edge triggered) a better chance of sampling correctly the narrow peaks (1/8th of the bit rate) of the OCDMA decoded signal.

The 1:16 deserializer converts the RZ signal with 1/8 duty cycle to an OC-3 NRZ signal. The deserializer also produces a 155.52 MHz clock by dividing the clock output of the CDR by 16. The controller is needed to determine which of the 16 output ports of the deserializer should be steered to the output of the OCDMA receiver when the link is first established. This is accomplished by monitoring and reframing the 16 outputs of the deserializer.

The OCDMA receiver can be used in OCDMA systems other that the one described here. The receiver supports chip rates of OC-3, OC-12, OC-48, Gigabit Ethernet (GbE), and 15/14 FEC rates. The supported bit rates depend on the number of time chips N in the OCDMA code and the availability of a 1:N deserializer. The design of the receiver can be easily upgraded to support 10 Gchip/s rates using commercially available components for OC-192 applications.

3. Measurement Results

Fig. 2(a) illustrates the 3 encoded optical signals (measured with an optical sampling module having a 12.5 GHz bandwidth). Fig. 2(b) confirms that the reconstructed desired signal (auto-correlation peak) is indeed distinguishable from the MAI. The cross-correlation pulses in the decoded waveform correspond to the interfering wavelengths that are retained by the decoder.

Fig. 2(c) shows the signal after the photoreceiver, which has an 800 MHz bandwidth. The output of the OCDMA receiver, after 3R regeneration, is shown in Fig. 2(d). This is the recovered clock and data when all three users are transmitting. The measured root-mean-square (RMS) jitter on the recovered clock is 15.6 ps (0.002 UI rms). The receiver not only recovers the clock from the OCDMA signal; it also converts the multi-level RZ signal with a duty cycle of 1/8 to an OC-3 NRZ signal.

The OCDMA receiver sensitivity with only the desired user transmitting is -19.1 dBm at a BER $\leq 10^{-10}$ using a PRBS of length 2²⁰-1. The introduction of one and two interferers causes power penalties of 2.8 dB and 9.9 dB, respectively. Fig. 3 shows the eye diagram after O/E conversion (signal "Z" in Fig. 1) with all three users transmitting. Note that the sampling oscilloscope was triggered at the chip rate in Fig. 3, whereas it was triggered using the pattern sync signal from the pulse pattern generator in Fig. 2(c). Finally, with only the desired user transmitting over 7 km of single-mode fiber (with no dispersion compensation), a power penalty of 3.6 dB is incurred relative to the back-to-back case.

4. Conclusions

In summary, we have described a multi-user OCDMA system demonstrator with full CDR using a novel OCDMA receiver, designed using commercially available components. No global clock was used in the system. The receiver functionality was demonstrated in a 2D λ -t OCDMA system, but can be used in other OCDMA systems. Furthermore, it allows digital logic circuits to process OCDMA data in the same way as if TDMA or WDMA had been used in the transport network. These results show the viability of OCDMA as a transport technology for access networks.







Fig. 3. Photoreceiver output at receiver sensitivity (-9.2 dBm) with all three users transmitting [signal "Z" in Fig. 1].

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