Design of a Fully Integrated Array of High-Voltage Digital-to-Analog Converters

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Abstract— The first fully integrated array of High Voltage (HV) Digital-to-Analog Converters (DACs) was designed in DALSA Semiconductor's 0.8um CMOS/DMOS HV process technology. The 6-bit 300V DACs are based on a current-steering, thermometer coded architecture and show a DNL of 0.16 LSB and an INL of 0.18 LSB. The current-to-high-voltage conversion is done using a high-compliance current mirror adapted to the HV technology, as traditional output resistor or op-amp solutions are not optimum for the HV process. The design is suited for applications requiring a set of digitally-controlled high-voltage signals.

I. INTRODUCTION

The number of transistors on integrated circuits (IC) has been on the rise since its inception. Though IC sizes may grow, the trend has resulted in the reduction in feature size of the integrated components. This scaling of technology results in advantages of increased speed, lower operating voltages and therefore lower power consumption. However, many applications require high voltages, notably intelligent motor control, biomedical applications, and optical switches including MEMS and electro-optic devices.

System integration of high voltage, analog and digital circuitry on a single die becomes attractive for these applications, as this results in reliability, cost and size improvements. Digitally controlling the high-voltage (HV) signals lays the foundation for the miniaturization of many devices. For this purpose, this paper proposes the first fully integrated array of HV digital-to-analog converters (DACs) operating from 0V to 300V. In our case, the DAC array will be used for electro-optic (EO) switching applications, though it is designed to accommodate a wide range of applications. The EO device will be flip-chipped to the CMOS chip, thus creating a fully packaged EO switch along with its associated drive electronics. The DAC and chip architecture is presented in section II followed by an overview of the HV process technology in section III. Section IV addresses the current-to-high-voltage (I-V) conversion. Finally, simulation results are discussed in section V, followed by test and measurements in section VI and the conclusion in section VII.

II. ARCHITECTURE

Optical simulations have shown that a 6-bit DAC provides a suitable voltage resolution for the desired optical performance of the EO switch. The overall chip architecture is shown in Fig.1. The ASIC consists of 64 HV DACs. In order to provide the 6-bit digital inputs to each DAC, 384 input pads would normally be required. This unrealistic port count is overcome by using a scan chain, shown in Fig.2, thus requiring only one input pad for the digital inputs.

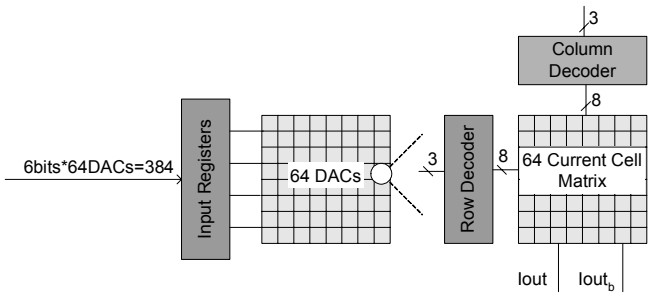

Figure 1. Chip architecture

Current-steering converters were chosen for these HV applications as they are faster and more linear [1] than other topologies in addition to being well suited for CMOS technology. Thermometer coded architectures are typically used for low-bit accuracies, such as in our 6-bit case. This implementation requires 2^6 current sources, each connected to digital logic, as in Fig. 3.

The digital signals come from a binary-to-thermometer encoder, depicted in Fig.1 as the row and column decoders. When the 6-bit input is increased by

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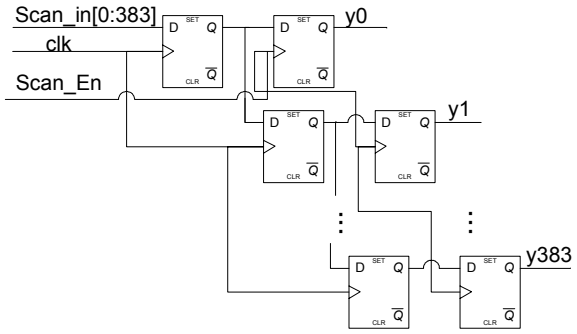

Figure 2. Scan-in chain

1 least significant bit (LSB), an additional current source in the cell array matrix is turned on, thus ensuring monotonicity, low glitch energy and relaxed matching requirements on the current sources (compared to a binary weighted DAC) [2]. The currents are then summed before undergoing current-to-voltage conversion. In contrast, in a binary weighted DAC, every switch switches an output current that is twice as large as the previous LSB. Though this architecture may be simple, a larger differential non-linearity (DNL) error ensues and the overall static and dynamic performances of the converter are compromised.

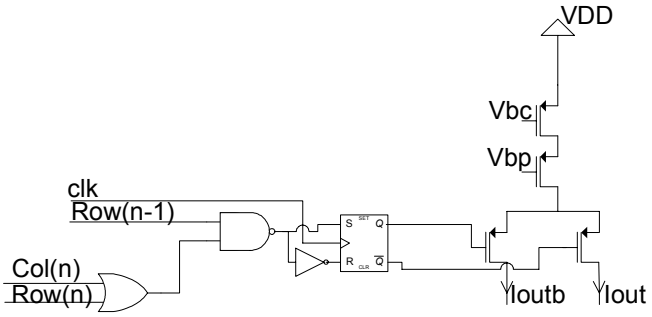

Figure 3. Current cell

III. HV TECHNOLOGY

Double Diffused Metal Oxide Semiconductor (DMOS) transistors are the most popular means of obtaining high voltage integrated circuits. In order to combine low-voltage and high-voltage circuitry on the same chip, a technique called RESURF (reduced surface field) allows drain breakdown voltages of up to 600V [3], [4]. In an n-type DMOS device as in Fig.4, a lightly doped P-Top region inside the N-Well is used in between the P-base and the drain in order to withstand the high drain-source voltage. For high drain voltages, this extra P-Top layer will deplete the drift region from above while the substrate depletes it from below, thus greatly increasing the total N-well charge that may be supported [3].

The high voltage components have certain specifications that have some bearing on the design choices. The main parameter to affect the design is V_{GS}. For N-type transistors, the breakdown voltage is 15V (nominal is 5V) whereas for a p-type transistor, the V_{GS} must be larger than -16V (nominal -5V). Thus, assuming a p-type device attached to a 300V supply, its gate voltage will have to be between 295V and 300V. This becomes an important design challenge, as conventional I-V conversion (using op-amps) is no longer a straightforward approach. This is discussed in the next section.

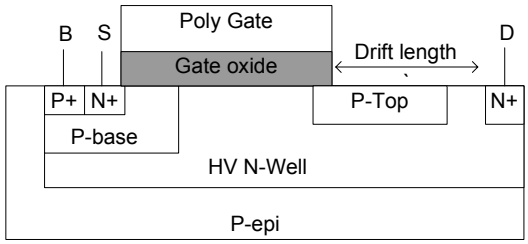

Figure 4. Cross section of HV NMOS device

IV. CURRENT-TO-VOLTAGE CONVERSION

The currents flowing from each current cell are summed to generate the total DAC current. Due to the high-voltage requirements, standard current-steering DACs, in which the I-V conversion is done using an output resistor or an op-amp, may not be applied. Fig.5 illustrates the former method.

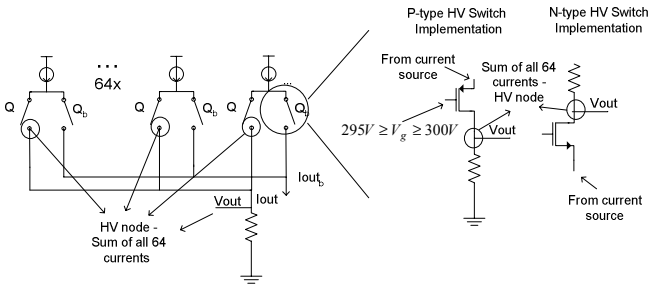

Figure 5. Current source array and transistor implementation for a single DAC unit.

This design is impractical because the current summation node would be a HV node, thus requiring all current switches in the current cells to be HV

transistors. The HV transistors are larger than regular CMOS transistors, such that utilizing 128 of these (for all current switches in an N-type realization of the switch) would require a large die size. Fig. 5 also shows the two alternative methods of implementing the current switches. In the N-type implementation, the main drawback is the elevated number of HV transistors, and therefore area, required. In addition to this problem, using the P-type alternative entails a method of providing the required gate voltages to these HV transistors, such as using level-shifters, and thus results in many more HV transistors. This is an important issue, as the overall chip will consist of 64 of these DACs. In addition, this can considerably slow down the settling speed of the converters. It is therefore crucial to circumvent this method of implementing the I-V conversion.

The op-amp solution is also difficult to implement due to the V_{GS} constraint discussed in the previous section. Fig.6 depicts a simple two-stage op-amp configuration. Transistors M1 and M8 must be high-voltage transistors in order to produce the desired HV signal. However, P-type HV transistors require that their gate voltage be within 5V of the source voltage. This constraint triggers a domino effect, in the sense that transistors M2 and M3 must now be HV transistors since their gates are connected to that of M1. This implies that I_{ref}, if implemented on-chip, would also consist of HV circuitry. It is therefore evident from this simple implementation that the output stage of a typical op-amp is not the optimal solution to provide the I-V conversion, as the area quickly increases with the number of HV transistors.

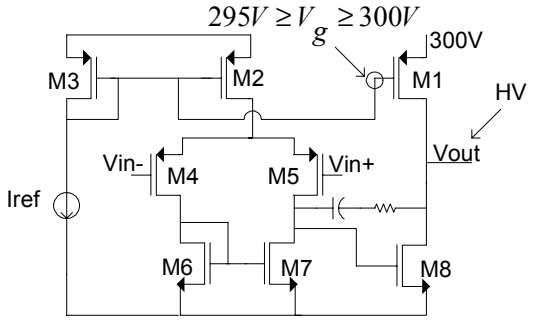

Figure 6. Two-stage CMOS op-amp implementation

One effective alternative is to use a high-compliance current mirror [5] and to replace the output transistor by HV transistors, as shown in Fig.7.

In this approach, the current is copied to the output node with a worst case error of 0.53 %, thus decoupling the current switches from the HV node. This particular implementation sources 2mA to a capacitive load. This technique considerably reduces the number of HV transistors in each DAC unit (from 128 to 6), and therefore results in a great savings in die area.

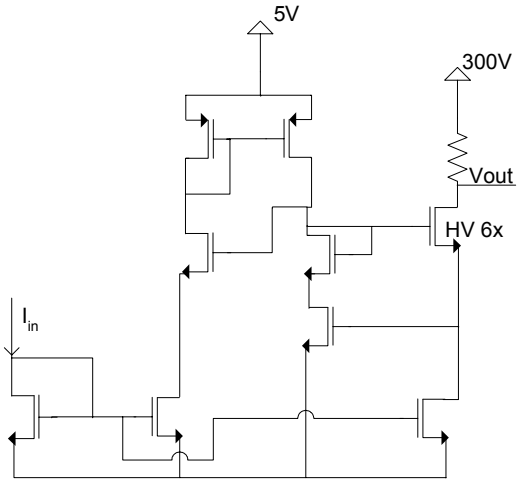

Figure 7. High output impedance current mirror

V. Simulation Results

The proposed HV DAC was designed in DALSA Semiconductor's 0.8um 5V/300V, quadruple well, three metal layer, epitaxial silicon process. The DAC was simulated using Spectre. Fig.8 shows the integral non-linearity (INL) profile versus input code and Fig.9 shows the DNL profile for the 6-bit converter over the 0 to 300V range. The INL lies between -0.18 and 0 LSBs whereas the DNL lies between -0.16 and 0.03 LSBs.

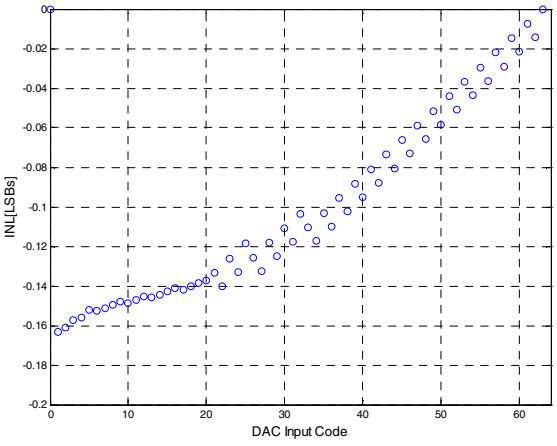

Figure 8. INL profile

The DAC's settling time, defined as the time to reach 1% of its final value was measured to have a worst case value of 8.7 µs, as shown in Fig. 10.

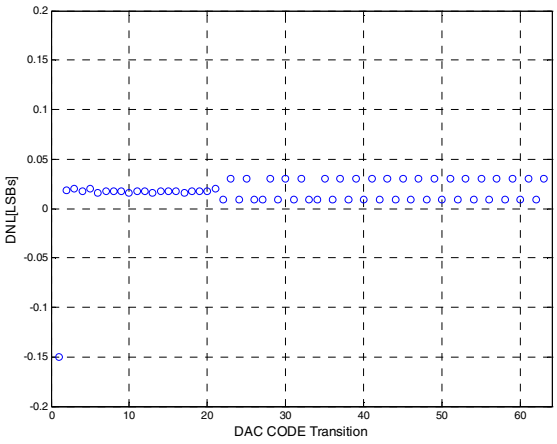

Figure 9. DNL profile

VI. TEST AND MEASUREMENT

The design was sent for fabrication in November and will be ready for testing in March 2005. Probe pads have been placed at various locations within the DAC to ensure proper debugging and testing of the pre-hybridized chip. Once the CMOS/DMOS chip has been heterogeneously integrated with the EO device through flip-chip bonding, a method of ensuring connectivity between the optical and electrical devices is provided. The chip requires a minimum of two flip-chip pads per electrode: one to provide the HV signal to the EO device from the DAC and the other to test connectivity. Since probing is no longer an option after flip-chipping, wire-bonding pads are used, thus allowing us to measure the voltages being sent to the optical devices while ensuring that the heterogeneous integration was successful. All the simulation results presented in the previous section were done using a capacitive load emulating the optical device. Experimental tests will be done to corroborate the simulation results. Results of experimental measurements will be presented at the conference.

VII. CONCLUSION

The design of a 6-bit 300V DAC for high-voltage applications was presented. The proposed HV DACs are based on a current-steering, thermometer coded topology tailored to DALSA Semiconductor's 0.8um CMOS/DMOS high voltage process technology. The high-voltage transistor limitations and their impact on design decisions were discussed. Simulation results of the HV DAC corroborate the viability of integrating electro-optic switches along with the associated electronics. The DACs offer good linearity, having a worst case DNL of -0.16 LSB and INL of -0.18 LSB over the 0 to 300V range, thus ensuring proper optical performance.

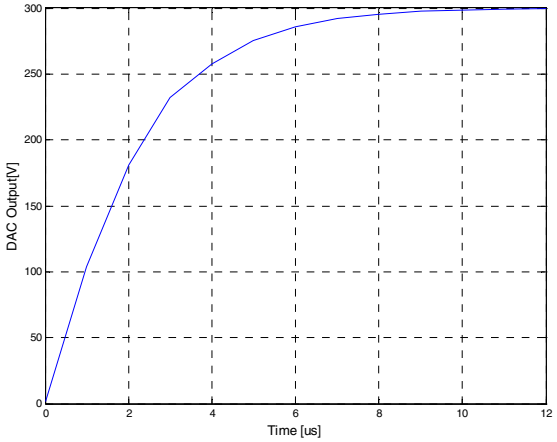

Figure 10. Simulation of HV DAC worst-case settling time.

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