A 24mW 2.5Gb/s VCSEL Driver in 0.18um CMOS

Jean-Philippe Thibodeau[1], Chris Murray[2] and David V. Plant[1]
[1]Department of Electrical and Computer Engineering, McGill University, Montreal, Canada
[2]Emcore Corporation, Albuquerque, New Mexico, USA

1 Introduction

With the ever increasing processing capacity of digital systems, electrical interconnects linking CMOS chips have become the limiting performance factor. Optical interconnects have been proposed as a promising alternative to increase interconnect capacity [1]. Although vertical-cavity surface-emitting lasers (VCSEL) are well suited for such an application [1], high-speed VCSEL drivers reported in the literature generally consume a significant amount of power [2,3]. In this paper, the design and testing of a 2.5 Gb/s VCSEL driver for short-to-medium reach optical interconnects is outlined.

2 Circuit design

The driver is designed in a TSMC CMOS 0.18um process made available through the Canadian Microelectronics Corporation (CMC). The system-level topology of the driver is illustrated in figure 1 [4]. A low-voltage-differential-signal (LVDS) is applied to the inputs of the pre-amplifier stage, implemented as a common-gate amplifier. The pre-amplifier has a gain of 11dB and a 3dB bandwidth exceeding 2GHz. The pulse-shaping stage further amplifies the signal and distorts it to prevent the current steering transistors of the laser driver stage from entering into full cut-off. This leads to better symmetry in the rise and fall times of the generated optical signal. The laser driver consists of a conventional current-steering differential pair with a dummy PMOS load in one of the branches. The resulting modulated current is combined with a bias current generated on-chip and pulled directly from the VCSEL. All stages are designed in NMOS with PMOS loads and biased at maximum f_T for optimum performance. A system simulation model, including models for the printed-circuit board (PCB) leads, ceramic quad-flat package (CFP) leads, VCSEL die, bond wire and extracted chip parasitics, was developed in Cadence and simulated using SpectreS. The simulated eye diagram of the current through the VCSEL is shown in figure 2(a) at 2.5 Gb/s. Although the driver can perform in excess of 5 Gb/s, laboratory experiments on the test fixture show eye closure and significant jitter around 3 Gb/s, which limit the performance of the system.

3 Experimental setup and measurement results

The fabricated driver chip was packaged in a CFP 80-pin package, along with a 10Gb/s VCSEL die provided by Emcore Corporation, and mounted on an RF test PCB. The VCSEL has a threshold current of 1mA and a slope efficiency of 0.5W/A. The LVDS input is applied with an Anritsu MP1763B pulse pattern generator through RF cables. The modulated optical signal is relayed to a New Focus 12GHz photoreceiver through a free-space two lens telecentric system with focal lengths of 15mm. In order to perform bit-error rate (BER) measurements, the photoreceiver output signal was further amplified with an RF amplifier. Eye diagram measurements were taken using a Tektronix 8000 communications signal analyzer. Measured eyes diagrams at 1.25Gb/s, 1.5Gb/s and 2.5Gb/s are provided in figures 2(b), 2(c) and 2(d) respectively. BER measurements at various pseudo-random bit sequence lengths for the three bit rates mentioned above along with power consumption measurements are included in table 1. BER measurements at 2.5Gb/s were unavailable at the time of submission due to measurement issues. Power consumption measurements include the VCSEL modulation and bias currents, which represent 75% of the total power consumption. The average optical power emitted by the VCSEL is 2mW at 2.5Gb/s. We expect to achieve better data rates and BER in the future by probing the inputs of the driver or using a higher bandwidth test fixture.

4 Conclusions

We have outlined the design and test of a 2.5Gb/s VCSEL driver in 0.18um CMOS. It consumes an average of 24.2mW at 2.5Gb/s for an average emitted optical power of 2mW, which compares advantageously with other published designs [2,3].

5 References

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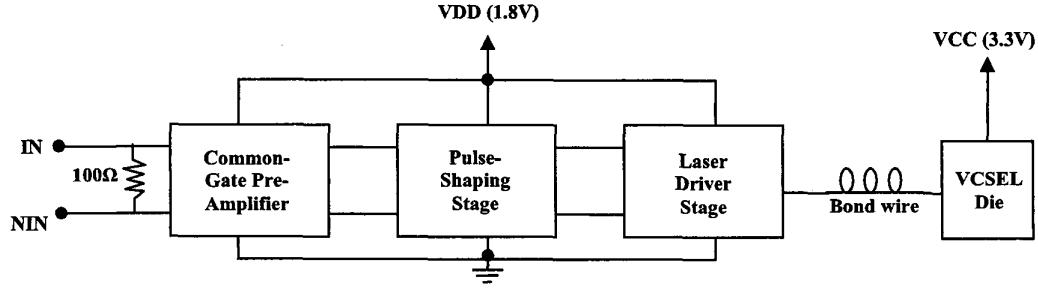

Figure 1: System-level topology of the VCSEL driver

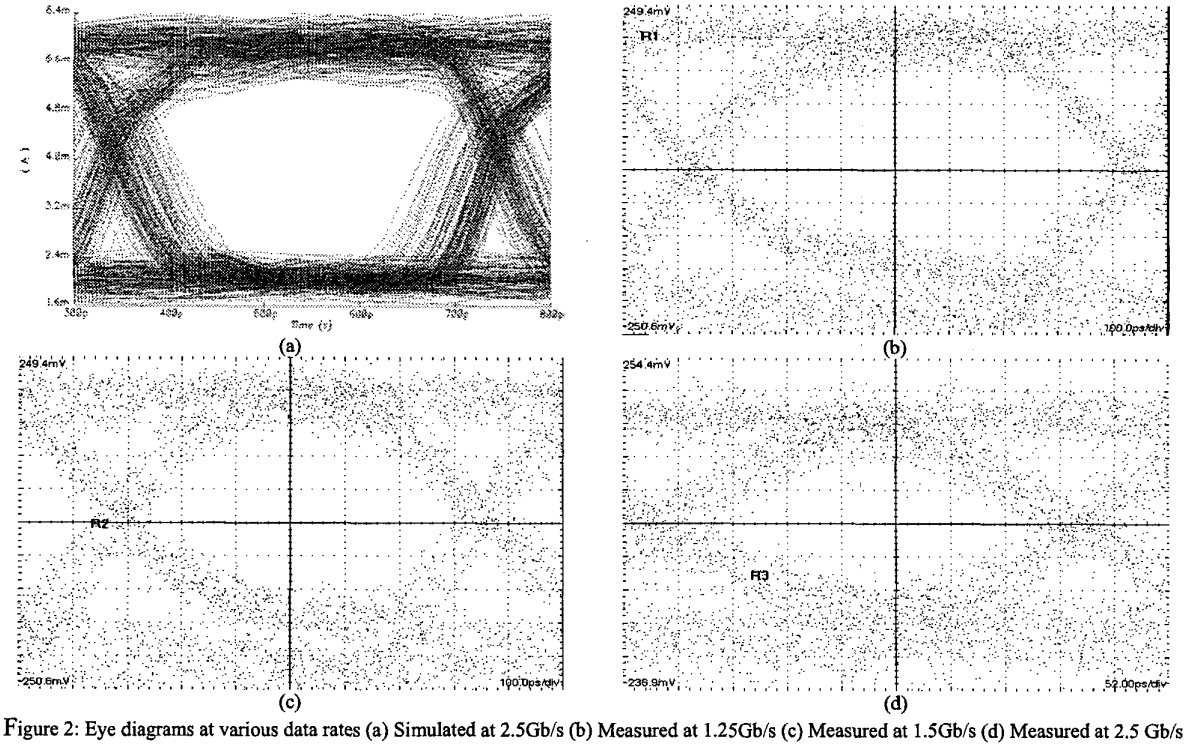

Figure 2: Eye diagrams at various data rates (a) Simulated at 2.5Gb/s (b) Measured at 1.25Gb/s (c) Measured at 1.5Gb/s (d) Measured at 2.5 Gb/s

Data Rate	PRBS Length	BER	Total Power Consumption
1.2 Gb/s	2^{31}-1	$< 10^{-10}$	19.8mW
1.5 Gb/s	2^{15}-1	$< 10^{-9}$	22.9mW
1.5 Gb/s	2^{9}-1	$< 10^{-12}$	22.9mW
2.5 Gb/s	TBD	TBD	24.2mW

Table 1: Bit-error rate and power consumption measurements for three data rates