Receiver operational yield in optoelectronic-VLSI applications

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ABSTRACT

It is well understood to be more difficult to operate an array of receivers simultaneously than individually, as sensitivity is degraded in the presence of simultaneous switching noise[1,2]. In optoelectronic-VLSI applications, additional operability concerns exist due to the need to implement receiver circuits of reduced complexity due to physical space constraints and to bias and control receivers in groups. Operational yield refers to the percentage of receivers in a group that can simultaneously be operated successfully. Receivers in a group may be functional individually, but some may exhibit operational problems such as duty cycle distortion or stuck-at 1/0 behavior when operated as a group. The transfer characteristics of optically single-ended receivers can be sensitive to changes in biasing and control parameters. If a sensitive parameter is common to a group of receivers, operational yield can be compromised by problems caused by process variations in optoelectronic devices and in transmitter and receiver circuits, and non-uniformity in optical system power throughput. We present experimental and simulation-based analyses of operational yield for optically single-ended receivers in common bias and control groups. Architectures employing optically differential signaling are shown to facilitate approaches to alleviating operational yield problems.

Keywords: CMOS, parallel optical interconnects, optoelectronic-VLSI, optical receivers, optical transmitters

1 INTRODUCTION AND BACKGROUND

1.1 Limitations on receiver design in OE-VLSI

In dense optical interconnect applications such as optoelectronic-VLSI (OE-VLSI), optical connections can number in the hundreds or thousands, and generally involves large arrays of optoelectronic devices (OEDs) integrated with underlying CMOS VLSI circuitry using a heterogeneous integration procedure[2,3] such as flip-chip bonding. The OEDs are generally located directly above their corresponding transmitter or receiver circuits, and the OED pitch sets restrictions on the allowable transistor layout size for each circuit. Two-dimensional OED array pitches of 125 μm are readily feasible[2,4], and pitches of 62.5 μm and smaller are technologically possible from a manufacturing and integration perspective[5]. In optically single-ended architectures with one OED per transmitter or receiver, the maximum layout area available to implement a transmitter or receiver is approximately the OED pitch. In an optically differential architecture, the available layout area is approximately twice the OED pitch in one dimension and approximately equal to it in the other dimension.

These restrictions are particularly significant for the receiver, possibly limiting the circuit complexity that can be implemented. Receiver circuits for telecommunications applications are typically comprised of multiple stages, each dedicated to a particular circuit function such as the pre-amplifier, amplifier stages with automatic gain and/or offset control, voltage thresholding, clock/data recovery, and equalization. In such designs, it is common for discrete off-chip components such as capacitors to be employed to provide AC-coupling between receiver stages, and for on-chip discrete components such as resistors, capacitors and inductors to be used for various purposes such as the implementation of voltage averaging circuitry[6] or the provision of bandwidth enhancement features[7].

In OE-VLSI applications, off-chip discrete components are not a practical option due to the scale of the receiver array. Passive on-chip discrete components are generally too large to be used in the available area. For example, a receiver implemented in an OE-VLSI system using 0.35 μm CMOS technology[2] utilized a layout area of approximately 50 μm

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on a side for the entire circuit. A single poly-poly capacitor of the same dimensions would yield a mere 2 pF capacitance, which would be only marginally useful for voltage averaging purposes at most data rates of interest. In very high data rate applications, the use of on-chip inductors to provide bandwidth enhancement is common in high data rate applications. However, a single 8 nH inductor, which might be used for such purposes, can easily occupy a layout area of approximately 500 μm on a side[7], clearly making it inappropriate for use in OE-VLSI applications.

As a consequence of these restrictions, amplifier stages for OE-VLSI receivers should employ a conservative and simple design. Circuit stages that cannot be implemented as such should be avoided. Passive circuit elements should be implemented using active devices wherever possible, or eliminated altogether. For example, the pre-amplifier is often implemented as a simple common-source CMOS inverter using resistive feedback in the form of a MOS device operated in the triode region[2,8].

1.2 Common bias/control receiver groups

In OE-VLSI, there is a practical need to organize large arrays of transmitters and receivers into groups that are commonly biased and controlled to keep the total number of control inputs manageable and to conserve chip I/O pins. There is also a practical need to provide operational flexibility for the circuits in the array by allowing parameters such as the magnitude of the feedback resistance for the receiver pre-amplifier to be configurable. Operational flexibility allows problems arising from, for example, silicon or OED process variations or power throughput non-uniformity in the optical system, to be dealt with.

1.3 Receiver operational yield

Operational yield is defined as the percentage of receivers in a common bias/control group that be operated at a desired data rate with a desired bit-error rate. It is possible for receivers in the common bias/control group to be able to meet a given set of performance criteria individually, but to fail to do so when all receivers in the group are simultaneously operated.

Imperfect receiver operational yield can be due to dynamic operational problems such as the presence of additional simultaneous switching noise generated from neighboring receivers. This results in degraded receiver sensitivity and bit error rate, generally worsening as more receivers are simultaneously operated and as the data rate is increased. Imperfect receiver operational yield can also be due to static operational problems arising from insufficient operational flexibility provided by the common bias/control group, as will be discussed in later sections.

2 OPERATIONAL CHARACTERISTICS OF OPTICALLY SINGLE-ENDED RECEIVERS

2.1 Basic operation

The essential function performed by an optical receiver is to convert an optical input signal into an electrical output signal. In OE-VLSI, an optical receiver typically consists of a photodetector to convert the optical input signal into a photocurrent signal, a pre-amplifier stage to convert the photocurrent signal into a small-swing voltage signal, one or more post-amplifier stages to amplify the voltage signal and provide an optimal output DC voltage offset to the decision stage, which amplifies the voltage signal to the power and ground rails.

The photodetector and the various receiver stages are generally DC coupled, and the electrical transfer characteristic (TC) relates the output voltage to the input photocurrent, as is shown in figure 1 for a non-inverting receiver[2]. The TC transition region is bounded on both sides by ranges of input photocurrents that correspond to logic 0 and logic 1 outputs. The transition region corresponds to the range of input photocurrents for which the receiver exhibits an indeterminate or intermediate logic state. At the center of the transition region, midway between the power and ground rails is the optimal operating point, and corresponds to an optimal average input photocurrent, denoted I_{OPT}. For any set of configurable parameters such as power supply and pre-amplifier feedback resistance magnitudes, there will be a corresponding TC, transition region location, and I_{OPT}.

2.2 Operational success/failure at a given data rate

From a qualitative operational perspective, the degree to which the average input photocurrent coming from the

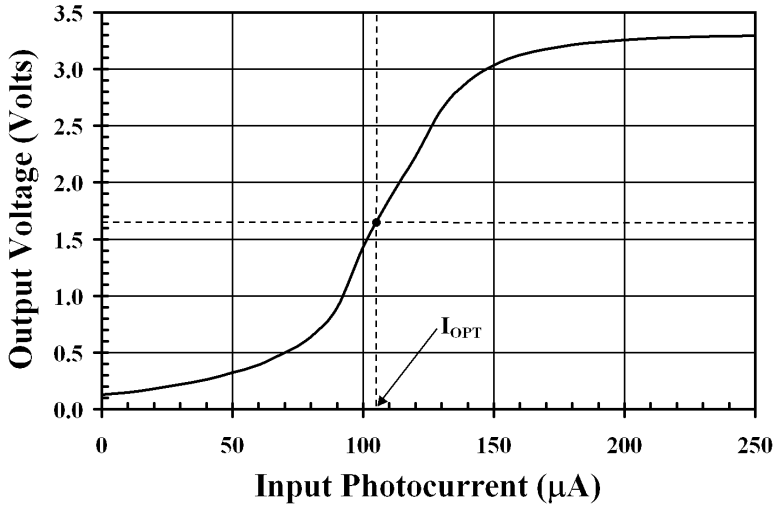

Figure 1. Representative transfer characteristic of a single-ended receiver[2]

photodetector (denoted I_{AVG}) deviates from I_{OPT} strongly determines whether an optical receiver is operating successfully, the degree to which it is operating successfully but imperfectly, or whether it is not operational at all. Other influential factors include the input photocurrent swing, denoted Δi_{PH}, and the width of the transition region of the TC, denoted ΔI_{TC}, which represents a crude measure of the sensitivity of the receiver.

Under ideal conditions, I_{AVG} and I_{OPT} coincide, and Δi_{PH} is larger than ΔI_{TC}. In such a situation, the input photocur-

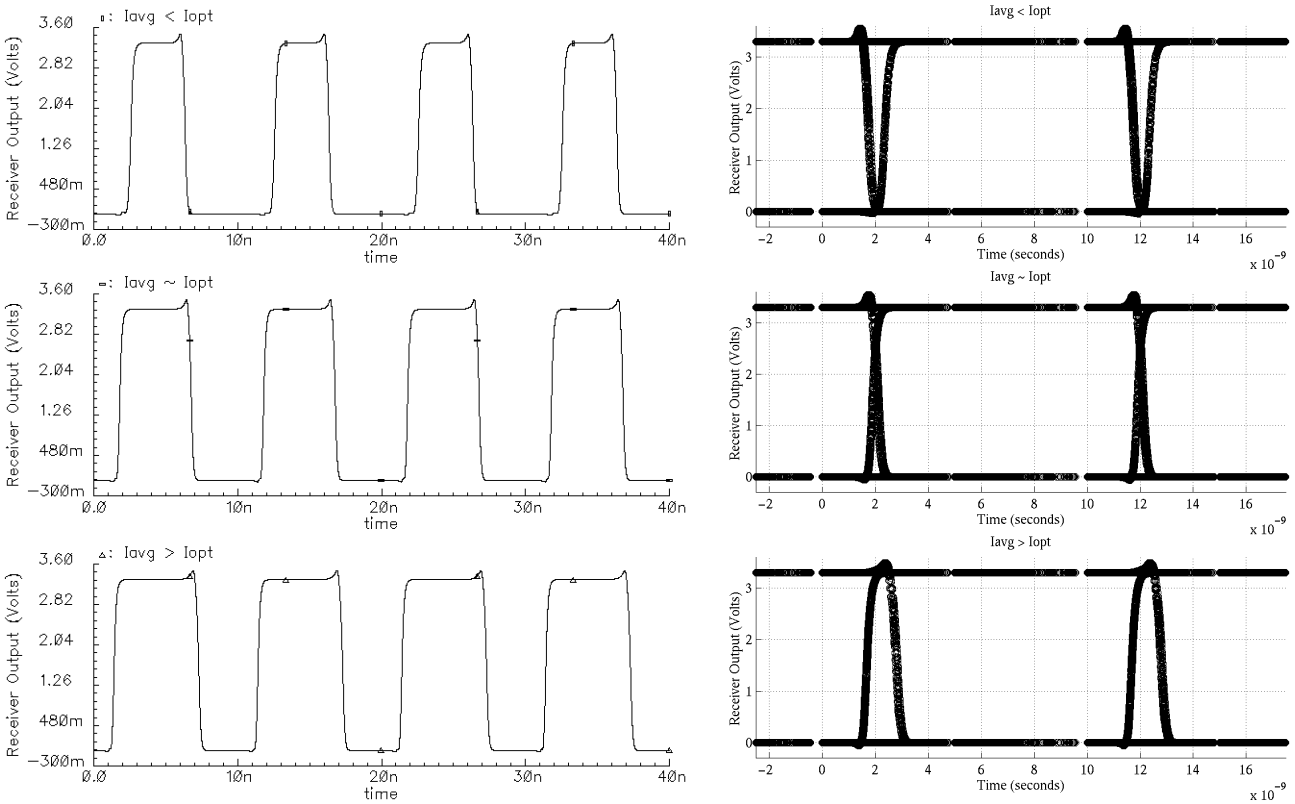

Figure 2. Receiver simulation at 100 Mb/s illustrating the effects of the magnitude of I_{AVG} relative to I_{OPT}. Left-hand side: square wave input-output symmetry (middle) and duty cycle distortion (top and bottom). Right-hand side: corresponding eye diagrams.

rent in the logic 1 and 0 states extend symmetrically beyond either edge of the transition region of the receiver TC. The resulting receiver output signal will exhibit a perfect duty cycle and an optimum eye diagram. When I_{AVG} is smaller than I_{OPT}, the input photocurrent in the logic 0 state extends farther beyond the edge of the receiver TC than it does in the logic 1 state. Correspondingly, when I_{AVG} is larger than I_{OPT}, the input photocurrent in the logic 1 state extends farther beyond the edge of the receiver TC than it does in the logic 0 state. In both cases, the resulting receiver output signal will exhibit duty cycle distortion and an eye diagram with a smaller eye width. The degree to which Δi_{PH} is larger than ΔI_{TC} determines the severity of the duty cycle distortion and eye diagram degradation. As Δi_{PH} approaches the magnitude of ΔI_{TC}, the problem worsens. In the event that I_{AVG} deviates too far from I_{OPT}, the receiver can exhibit stuck-at 1 or 0 behavior.

Some of the scenarios described above are illustrated in figure 2, where an OE-VLSI receiver[2] was simulated with a photocurrent input signal at 100 Mb/s with constant bias and control settings to maintain a constant I_{OPT}, with different simulations performed for different I_{AVG} conditions relative to I_{OPT}. The left hand side waveforms represent the receiver outputs in response to a square wave input, while the right hand side waveforms are simulated eye diagrams of the receiver output in response to a pseudo-random bit sequence (PRBS) of length 2^9-1. The middle portion of figure 2 represents the condition $I_{AVG} \approx I_{OPT}$, with the receiver output showing minimal duty-cycle distortion and a nearly perfect eye opening. The top and bottom portions of figure 2 show the duty cycle distortion present in the output and the resulting reduction in eye opening for the conditions $I_{AVG} < I_{OPT}$ and $I_{AVG} > I_{OPT}$, respectively.

2.3 Operational success/failure as a function of data rate

As data rates increase and approach the bandwidth of the receiver, the operational problems described in the previous section for a given data rate become worse as a result of the effective widening of the transition region of the receiver TC due to the reduced amount of gain available from the receiver at higher data rates. This effectively results in reduced receiver sensitivity and a reduced difference between Δi_{PH} and ΔI_{TC}, causing the duty cycle distortion problems arising from a mismatch in I_{AVG} and I_{OPT} to become more severe. Duty cycle distortion present in the receiver output at a lower data rate can become stuck-at-1/0 behaviour at a sufficiently high data rate.

In an OE-VLSI environment, it is well known that the presence of simultaneous switching noise on the power supply rails will detrimentally affect receiver operation[1], worsening as the data rate is increased. It is also known that the TC

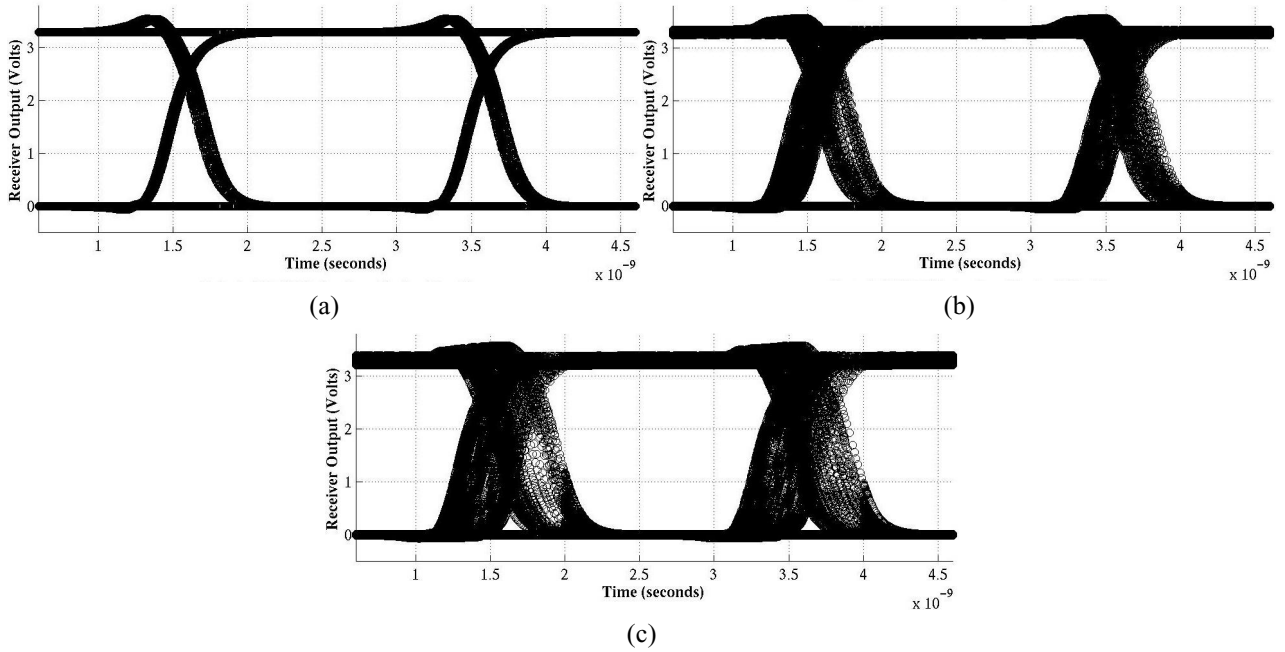

Figure 3. Simulated receiver eye diagram at 400 Mb/s illustrating effects of power supply noise on receiver operation. (a) 0 mV noise amplitude (b) 50 mV noise amplitude (c) 100 mV noise amplitude.

of a receiver can be affected by changes in the supply voltage. This approach has been explicitly used as a means of performing crude offset control in a receiver to achieve optimal operation for a given I_{AVG}[8]. Thus, from an operational perspective, switching noise on the power supply rails results in corresponding time-domain shifts in the transition region of the receiver TC, effectively resulting in an increased ΔI_{TC} and an ambiguity in the magnitude of I_{OPT}. This is illustrated in figure 3, which shows simulated eye diagrams for an OE-VLSI receier[2] operating at 500 Mb/s, stimulated with a PRBS of length 2^9-1 under nominal $I_{AVG} \approx I_{OPT}$ conditions. Figure 3 (a) represents the idealized condition of no power supply switching noise and a very open eye diagram. Figure 3 (b) represents the condition where a 50 mV amplitude sine wave at 647 MHz is superimposed on the VDD supply, clearly resulting in a thickening of the portion of the eye diagram representing the logic 1 state, and a reduction in eye opening width. Figure 3 (c) represents a similar supply noise condition with 100 mV amplitude, and an eye diagram that is correspondingly further degraded.

2.4 Transfer characteristic problems in common bias/control groups

Receivers that are part of a common bias/control group are nominally set to have identical TCs and an identical I_{OPT}. In order to obtain operation of the entire group of receivers with minimal duty cycle distortion and optimal eye diagrams, it is necessary to provide each receiver in the group with the same I_{AVG}, and for it to be coincidental with I_{OPT}. This leads to the notion of a group TC, group I_{OPT}, and group I_{AVG}, as well as two corresponding problems from an operational perspective.

2.4.1 Problem #1: group transfer characteristic

In practice, the individual TCs in a common bias/control group will not be identical for a multitude of reasons. Figure 4 shows the measured TCs of a number of receivers of identical design[2] and in close physical proximity (less than 200 μm separating any two receivers). Clearly, I_{OPT} is not the same for all TCs, and can be attributed to the effects of silicon process variations. As mentioned previously, the TC of a receiver can also be affected by changes in the value of the supply voltage. Despite being nominally identically biased, it is possible for the power distribution network in a common bias/control group of receivers to be sufficiently resistive for IR voltage drops to cause localized supply voltage and TC variations for the receivers in the group.

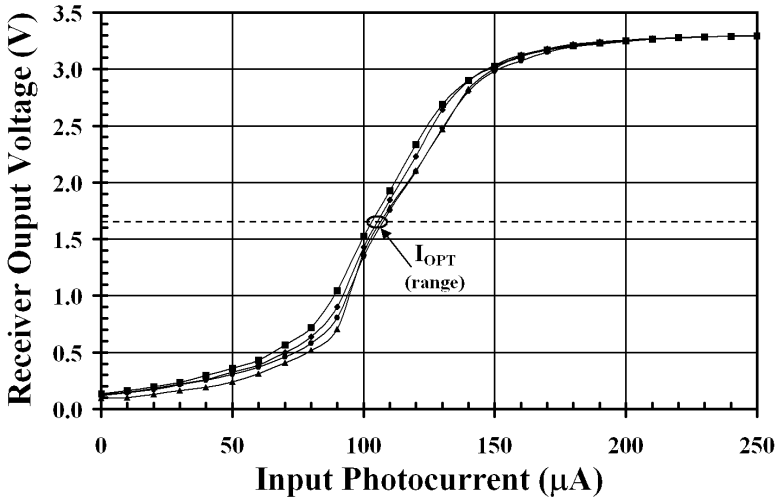

Figure 4. Measured TCs for multiple receivers of identical design, illustrating effects of silicon process variations on the receiver TC.

For a common bias/control group of receivers, the cumulative effects that result in individual TC variations establishes a *region of ambiguity* for I_{OPT} in the group TC. From an operational perspective, this manifests itself as a wider effective transition region for the group TC and correspondingly degraded group sensitivity over that of any individual constituent receiver. This is notwithstanding the result obtained by Woodward et al.[1] where the presence of simultaneous switching noise from an array of operating receivers caused the sensitivity of any individual receiver to be degraded. In both cases, it is necessary to operate the receiver array with increased Δi_{PH} by boosting optical power levels.

2.4.2 Problem #2: group average input photocurrent

As was mentioned previously, it is required to provide the same nominal I_{AVG} equal to the nominal group I_{OPT} to all receivers in a common bias/control group in order to achieve optimal operation across the group. From a practical perspective, it is beyond the control of the circuit designer to maintain uniformity in I_{AVG} across a group of receivers. In practice, the configurable parameters for a common bias and control group are typically modified to tweak the group TC to obtain optimal receiver operation across the group for a given set of operating conditions.

The degree to which I_{AVG} varies across the receivers in the group is determined by a multitude of factors, including the uniformity of the properties of the transmitter circuits and lasers that are used to generate the optical signals incident on the group of receivers, the uniformity of the properties of the photodetectors attached to the group of receivers, and the throughput uniformity of the optical system that is used to deliver the transmitted optical signals to the group of receivers.

There have been numerous studies on the uniformity of relatively small (8×8) arrays of VCSELs and photodetectors indicating that high degrees of uniformity are possible but, to the knowledge of the authors, no study has been performed for truly large (e.g. 32×32) arrays of OEDs. One study for an 8×8 array of oxide-confined VCSELs showed that variations from the mean in threshold current and output power (at 8 mA bias) as small as ±3% and ±1.5%, respectively could be achieved[9].

Large-scale optical imaging systems generally suffer from poor power throughput uniformity. A clustered micro-optical system designed to relay 512 optical beams arranged as 32 4 x 4 clusters of beams was found to have power throughput variations from the mean of ±35% within a typical cluster[10]. Another optical system for an 8 x 8 array of optical beams based on a fiber image guide with 10μm diameter fibers and 1.4μm claddings was found to exhibit power throughput non-uniformity between ±10% and ±35%, depending on the size of the input spot radius[11].

The problem with having a non-uniform I_{AVG} across a common bias/control group is that the group I_{OPT} cannot be made optimal for all receivers simultaneously. The severity of mismatch in I_{AVG} across the group will determine the degree of operational problems that result. The less uniform that I_{AVG} is, the greater the chance of duty-cycle distortion or stuck-at 1/0 behavior and a corresponding reduction in operational yield to occur.

2.5 Operational yield example: DARPA/ARL VLSI-photonics program, demo #1[2]

The example given in this section discusses the design of an optically single-ended receiver on a chip fabricated in 0.35 μm CMOS technology for a system that implemented a 256 channel bi-directional optical interconnect[2]. This section will describe the receiver design, the chip organization into common bias/control groups, as well as the achievable receiver performance individually and the operational yield of the common/bias control groups.

2.5.1 Receiver design

The transistor-level schematic of the receiver circuit is shown in figure 5. It comprises four stages, including the pre-amplifier, an offset correction stage, a post-amplifier stage, and a Schmitt-trigger stage. The pre-amplifier is imple-

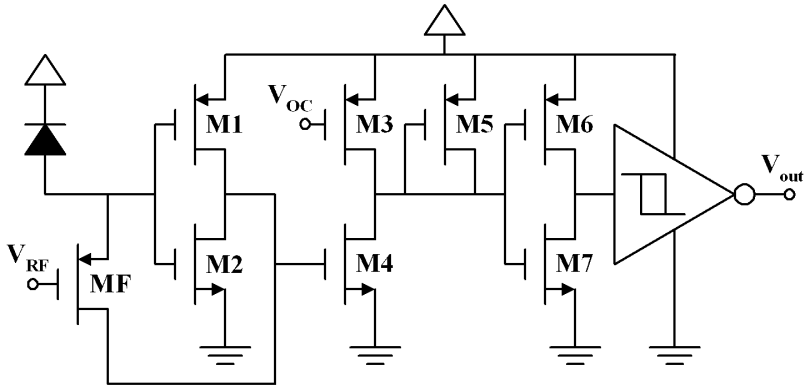

Figure 5. Transistor-level schematic of receiver implemented in DARPA/ARL VLSI-photonics program demo #1.

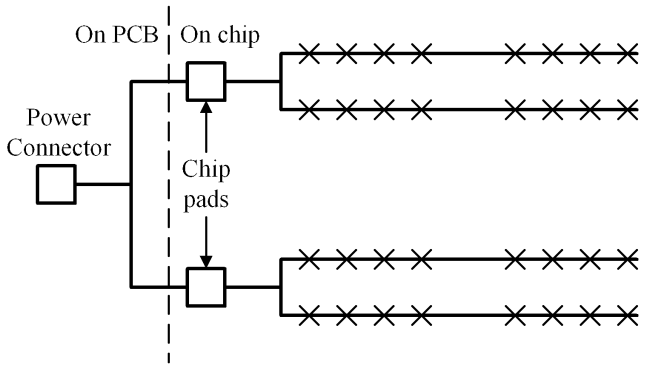

Figure 6. Illustration of power distribution network in a common bias/control receiver group. Individual receivers are indicated by "X".

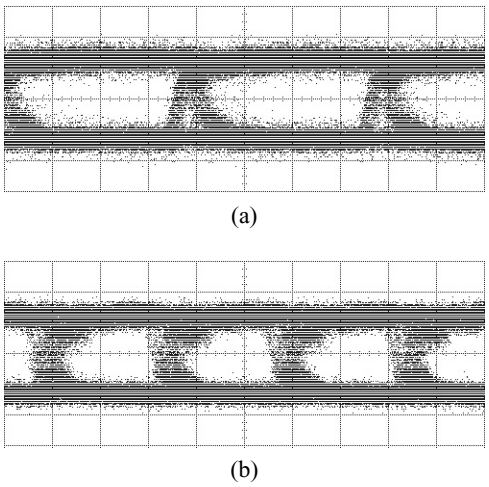

Figure 7. Eye diagrams of demo #1 receiver operating at (a) 250 Mb/s and (b) 400 Mb/s.

mented as a CMOS inverter (M1-M2) with a triode-mode PMOS transistor (MF) implementing tunable resistive feedback (control input V_{RF}). The offset correction stage is implemented as a common-source amplifier with diode connected load (M4-M5) with a PMOS transistor (M3) used as a tunable bias current source (control input V_{OC}) that serves to set the output DC voltage offset independently of the input DC voltage offset produced by the pre-amplifier output in response to a given I_{AVG}. The post-amplifier stage is a simple CMOS inverter (M6-M7). The purpose of the Schmitt-trigger is to introduce hysterysis in the final stage of the receiver transfer characteristic to provide some immunity to switching noise on the power supply rails. When referred back to the input, the hysterysis effect on the overall receiver TC is minimal.

2.5.2 Organization into common bias/control groups

The receivers were organized into eight groups of 32 with all receivers in the group having a common power supply and ground, PD bias voltage, V_{RF} and V_{OC} inputs. Common bias/control groups were arranged in a 2×4 array on a horizontal and vertical pitch of 1.5 mm. Each common bias/control group consisted of a 2×2 array of receiver circuit clusters on a 750 μm horizontal and vertical pitch. Each circuit cluster consisted of eight receiver circuits arranged in a 2×4 array with horizontal and vertical pitches of 125 μm and 250 μm, respectively.

The layout of the power and ground networks for the common bias and control group are illustrated in figure 6. Individual receivers are indicated with an "X". Power and ground are distributed along 1×8 rows of receivers, with tracks for pairs of rows being brought to pads on the chip. On the printed circuit board designed for the chip, all of the pads used to provide power and ground, respectively, were shorted together for each common bias/control receiver group. From the perspective of the power distribution network, each of the four 1×8 rows receivers indicated in figure 6 are indistinguishable.

2.5.3 Receiver performance and operational yield

When operated individually, the receivers exhibited satisfactory operation at data rates as high as 400 Mb/s for numerous combinations of optical power levels and swings and corresponding control parameters. Figure 7 presents experimentally measured eye diagrams of the receiver operating at 250 Mb/s and 400 Mb/s in response to a PRBS optical signal of length 2^8-1.

The correspondence between operational yield and data rate for the common bias and control group of receivers was investigated by illuminating all of the receivers in the common bias/control group with identical 2^8-1 PRBS optical data from a corresponding 32-element laser driver array passing through an optical system consisting of custom bulk lenses. All laser drivers in the array were set to provide the same nominal optical power levels in each logic state. For any given nominal optical power setting across the laser driver array, V_{RF} and V_{OC} for the common bias/control receiver group were tweaked to provide the maximum number of simultaneously operating receivers. A liberal qualitative measure was

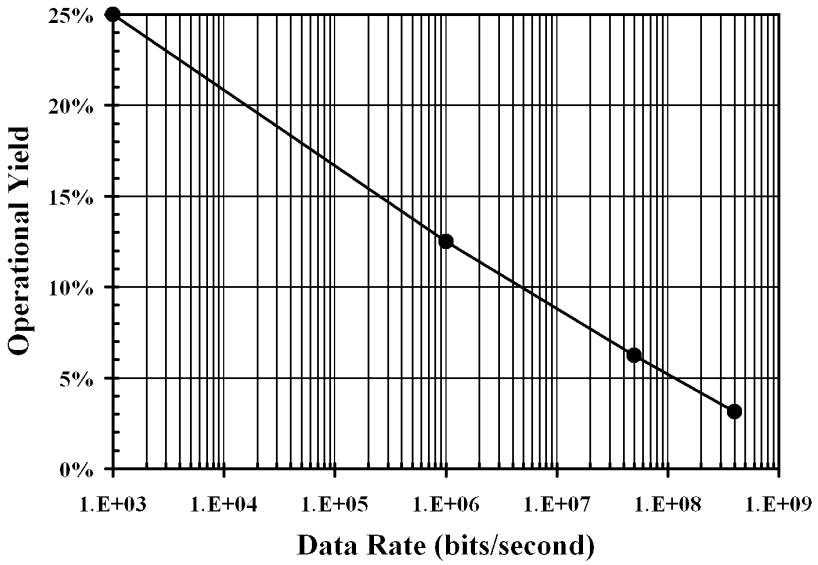

Figure 8. Experimental operational yield results for common bias/control receiver group.

used for successful operation – obtaining an eye diagram with an opening of at least one half the bit period width and one half the voltage swing height. Figure 8 presents the best results obtained from several combinations of laser driver output power and V_{RF}/V_{OC} settings for each data rate. Operational yield was found to be poor at any data rate (≤ 25%), and suggests that the power uniformity of the optical signals incident on each receiver in the group was poor and the group as a whole had poor tolerance to such non-uniformity. Further, operational yield worsened with increasing data rate by approximately 4%/decade, which is attributable to poor switching noise rejection capability of an individual receiver and the substantial amounts of switching noise present on the power supply rails, increasing as the data rate is increased.

These behaviours were confirmed via simulation. Simulations were performed on one of the indistinguishable 1×8 rows of receivers illustrated in figure 6 and described in section 2.5.2, modeling the resistive and capacitive elements of the on-chip power distribution network, and including the bonding wire implementing the off-chip connection. A PRBS of length 2^{9-1} was implemented as a piece-wise linear voltage source, with the data inputs to each receiver derived from it. I_{AVG} for each receiver was varied from 45 μA to 65 μA along the row of receivers, representing approximately a ±20% variation from the mean, and can be considered conservative based on the discussion of optical system throughput non-uniformity in section 2.4.2. Δi_{PH} was kept constant at 50 μA for each receiver. A single receiver circuit was simulated to determine optimal V_{OC} and V_{RF} control settings for these conditions, which were subsequently used for the entire 1 x 8 row of receivers. Switching noise was modeled by adding separate sinusoidal noise generator waveforms of different frequencies on the power and ground nets for the receiver group. Simulation results are shown in figure 9 at 400 Mb/s, corresponding to the maximum-targeted data rate for the receiver during design. The left and right-hand sides of the figure show simulation results when the amplitudes of the sinusoidal noise generators were set to 0V and 100mV, respectively. With no noise generation, the eye diagrams of some of the receivers are affected fairly severely by duty cycle distortion – qualitatively, 5 to 6 receivers are operating acceptably with an eye width opening of at least one third of the bit period. With noise generation included, this number is reduced to 2 to 3.

3 SOLUTIONS USING OPTICALLY DIFFERENTIAL RECEIVERS

The general solution to the operational yield problems presented in section 2 is to avoid receiver designs where the TC is sensitive to changes in any bias voltages or control inputs. In this manner, the operational yield of a common bias and control group of receivers at any data rate can be maximized. For the receiver design presented in section 2.4, the V_{OC} input and offset correction stage would have to be avoided, but at the same time an offset correction function, preferably on a per-circuit basis, must somehow be maintained. In a telecommunications receiver, this would normally be

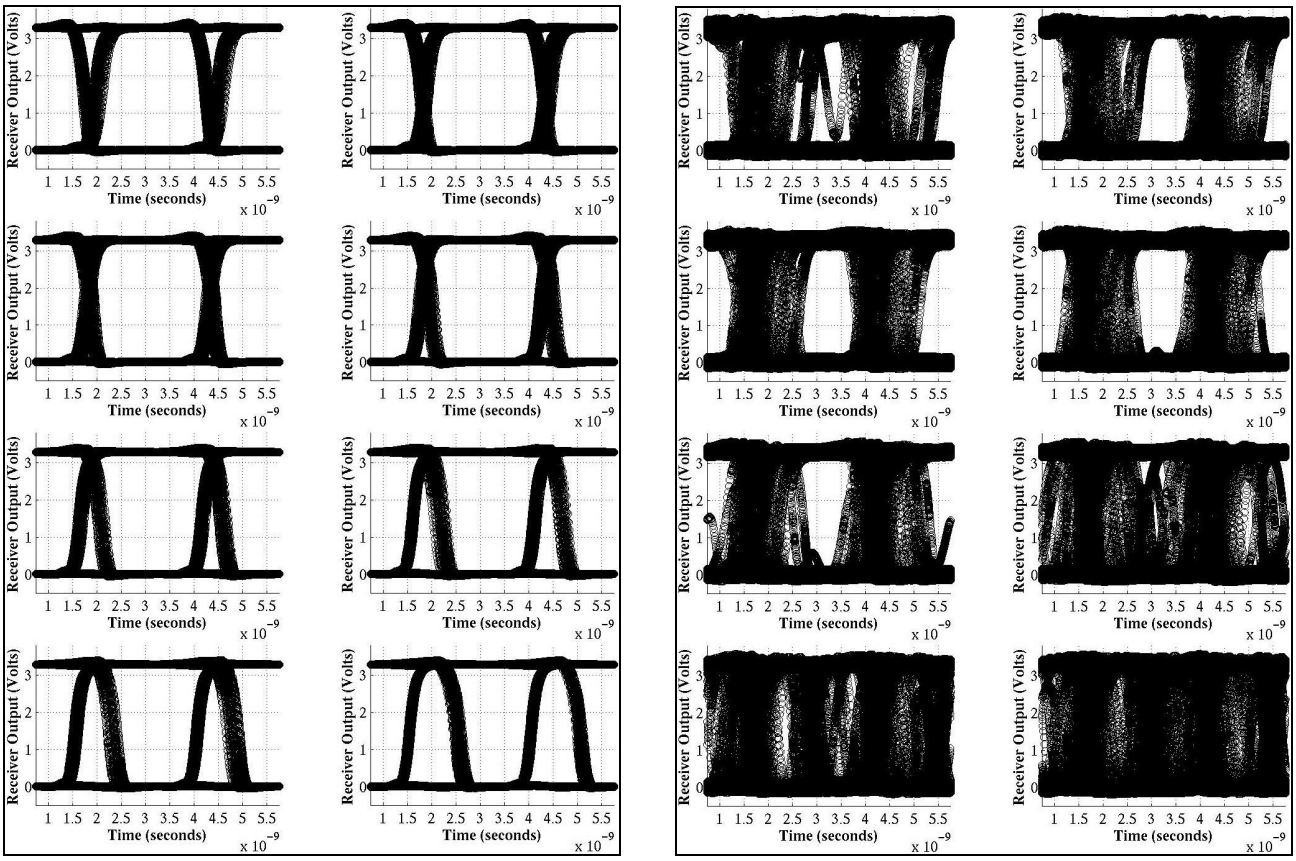

Figure 9. Simulated eye diagrams for a 1 x 8 row of common bias/control demo #1 receivers operated with a ±20% variation from the mean in I_{AVG}. Left-hand side: no power supply noise generation. Right-hand side: 100mV amplitude power supply noise generation.

implemented using some form of automatic offset control (AOC) circuitry. However, such circuitry typically requires the use of relatively large valued resistors and/or capacitors, and is likely to be unsuitable for implementation in an OE-VLSI environment. Further, the results of section 2.5.3 clearly illustrate the detrimental effects of switching noise in single-ended receivers, particularly at high data rates and under non-ideal I_{AVG} operating conditions.

Implementing an electrically differential receiver architecture is a possible means to improve the noise rejection capability of the receiver, and is fairly common[4,12]. It has been shown that the optimal architecture for providing maximum immunity to the effects of switching noise is one based on differential optical signaling and the use of fully differential transmitter and receiver circuits[12]. This approach both minimizes the generation of switching noise by transmitter and receiver circuits and maximizes their immunity to switching noise on the power supply. It also provides a means for the receiver to reject common mode switching noise imparted onto the optical output signals of a transmitter due to switching noise present on its power supply.

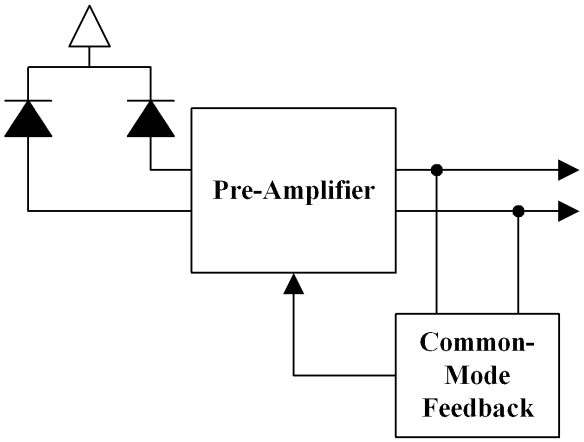

Figure 10. Fully differential pre-amplifier architecture with CMFB to effectively perform AOC.

In addition to providing maximum immunity to switching noise, a fully differential receiver architecture that employs differential optical signaling can be used to

implement what is essentially offset correction. Figure 10 shows the outline of such an architecture for the pre-amplifier, following that of an existing OE-VLSI receiver design[4]. The fully differential pre-amplifier has common-mode rejection and, in conjunction with the use of a common-mode feedback circuit, keeps the operating point stable and maintains the output DC offset in a narrow voltage range, effectively performing an AOC function.

3.1 Operational yield example: DARPA/ARL VLSI-photonics program, demo #2[4]

This section presents operational yield simulation results for an optically differential receiver implemented on a chip fabricated in 0.25 μm CMOS technology for a system that implemented a 540 channel optical interconnect[19]. The receiver comprises a fully differential pre-amplifier stage, two fully differential post-amplifier stages, and a line driver stage. Details of the design are omitted for brevity.

The operational yield behaviour of this receiver was investigated via simulation in a manner similar to that performed for the single-ended receiver discussed in section 2.5. Simulations were performed on a set of eight receivers with full modeling of the resistive and capacitive elements of the on-chip power distribution network, the bonding wire implementing off-chip power connections, as well as the interconnects driven by the line driver stages of the receivers. Simulation conditions are identical to those discussed in 2.5.3. Simulation results are shown in figure 11 at 250 Mb/s, corresponding to the maximum-targeted data rate for the receiver during design. The left and right-hand sides of the figure show simulation results when the amplitudes of the sinusoidal noise generators were set to 0V and 100mV, respectively. With no noise generation, the eye diagrams of all receivers in the common bias/control group are all exemplary. The addition of noise generation does not degrade the eyes of any of the receivers sufficiently to cause operational failures.

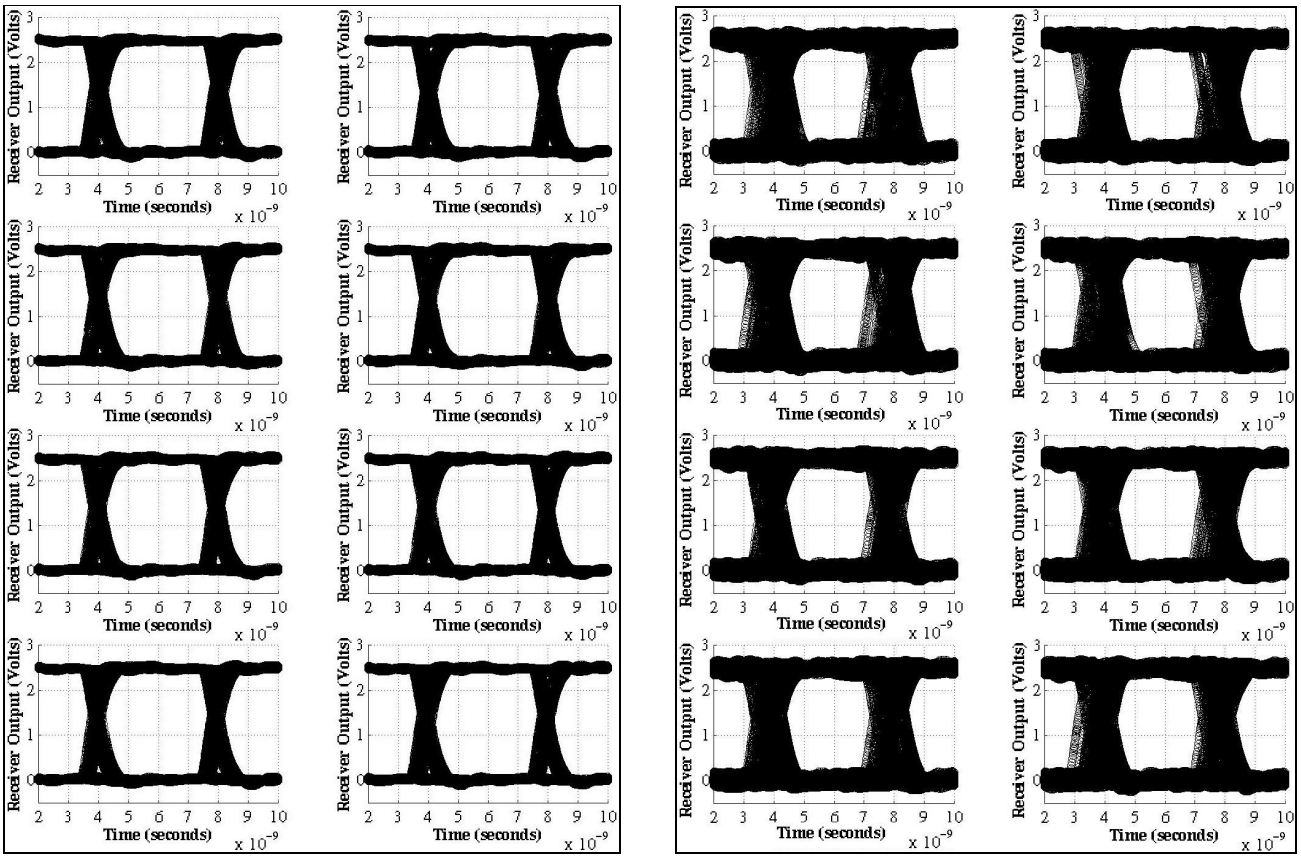

Figure 11. Simulated eye diagrams for a 1 x 8 row of common bias/control demo #2 receivers operated with a ±20% variation from the mean in I_{AVG}. Left-hand side: no supply noise generation. Right-hand side: 100mV amplitude supply noise generation.

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