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Design and Testing of a Smart Pixel Array for a Four-Stage Optical Backplane Demonstrator

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Introduction: Smart Pixel Arrays (SPA) can offer a large connection density at extremely high data rates for architectures such as switching fabrics and multiprocessor arrays (1). The SPA can take advantage of the surface to surface imaging capability of free space optics and the extremely low impedance loads of micron sized optoelectronics. An optical backplane could in principle provide a generic method with which these architectures could be implemented. In this paper, a dynamically reconfigurable interconnection mesh called the *Hyperplane* (2) was chosen to demonstrate the capabilities of an optical backplane system.

System Architecture: The system in which the SPAs are used constitute a representative portion of an optical backplane. Four printed circuit boards (PCB) are interconnected in a unidirectional ring via a single 4-bit wide channel using a hybrid optical relay (3). Each SPA has a 4-bit wide address associated with each PCB in the backplane and uses a "1-hot encoding" technique for the addressing scheme. This provides broadcast ability to the channel, and allows flexibility in the optical design by allowing for permutations in the bit order due to optical inversions of the relay system.

Logical Design of SPA: To allow complete testability of the initial design, the SPA is composed of only combinational logic. Each smart pixel within the array can be configured to either *inject* electrical data onto the backplane or *extract* electrical data from the backplane. In the extraction state, the smart pixel is also in an optically *transparent* state, allowing data to be retransmitted to the next stage.

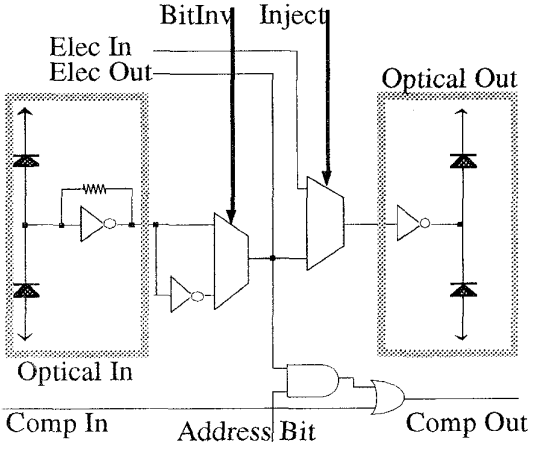

Figure 1: Logical description of Smart Pixel

The smart pixel is composed of dual-rail PiN receivers, and dual-rail MQW transmitters (4). The first multiplexer (MUX) provides a mechanism to correct for optical inversions of the dual-rail beams within the optical path (i.e.: a "high-low" pair of beams passing through a telecentric relay becoming a "low-high" pair of beams). A unique system measurement using this MUX can also be preformed. A *system level ring oscillator* can be produced by

placing all SPAs into a transparent state, and setting an odd number of inversions throughout the entire backplane using these MUXes. A sinusoidal waveform should be observed from the optical beam indicating the maximum frequency the backplane can maintain.

Because the numbers of bond pads along the perimeter of typical silicon chips is at a premium, some of the functions of the SPA have been placed into a 9-bit setup register containing the state of the MUXes, substantially reducing the number of bond pads. The photograph below shows the location of the register and the 4-bit channel of the SPA. Note that the SPA's channel has been centered about an optical axis to allow for an easier optical interconnect.

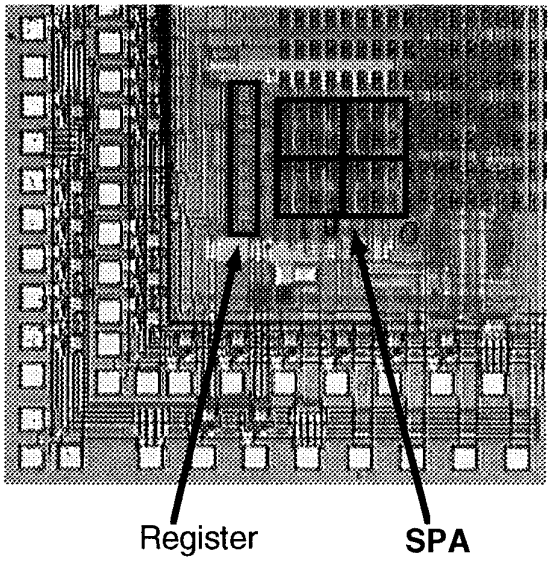

figure 2: Photograph of SPA

Electrical and Optical Testing: Before the SPA chip can be introduced into the backplane, several functional tests were carried out. The design required a set of peripheral electronics to operate the chip. A finite state machine was used to serially load the 9-bit register of the SPA, and to use the 4-bit bidirectional i/o port of the SPA chip effectively, a method of buffering the electrical i/o was implemented.

Initially, the peripheral electronics used a low bandwidth wirewrap board, and the SPA chip itself was placed in a PGA package interconnected with DIN ribbon connectors. The preliminary data using a two beam optical test rig showed that all three states of the chip worked with switching powers as low as 10μW for a bit rate of up to 2Mb/s in the extraction state (the nominal bandwidth limit of the wirewrap board).

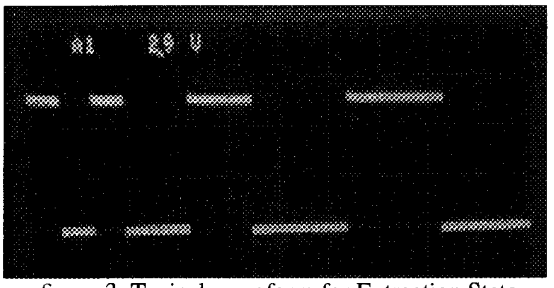

figure 3: Typical waveform for Extraction State

Custom microstrip PCBs are currently being built for both the peripheral electronics and the SPA. These boards will be integrated into the system and will allow the SPA to operate at much higher data rates. More complete measurements of the SPA will then be provided.

Conclusion: The initial characterization of a SPA for an optical backplane has been carried out. Initial measurements of the functionality and the performance have been done, and higher speed measurements will be carried out on custom PCBs. This design will then be incorporated into a four-stage optical backplane demonstrator.

References:

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