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A *HyperPlane* Smart Pixel Array for Packet Based Switching

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Abstract

The operation, simulation, and testing of a 4x2 CMOS-SEED smart pixel array is presented. The smart pixel array discussed implements a HyperPlane based ATM switch.

1. Introduction

A brief review of *HyperPlane*[1,2] packet based switching is presented. Then, details of the designed smart pixel array (SPA) are examined including smart pixel circuitry and transimpedance receiver design. Finally, the results of initial optical and electrical testing are reported and discussed.

2. A *HyperPlane* Based ATM Switch

In this switch, each user is assigned to one of the system printed circuit boards (PCBs). A corresponding SPA is located on each PCB, and each SPA is point-to-point optically connected to the SPAs on adjacent PCBs. Each SPA, and thus each user, is configured at start-up with a unique fabric address. For each node channel in the *HyperPlane*, a fixed transmitted assignment is utilized, so that only one SPA (user) may send packets on that node channel. All other SPAs (users) are configured to receive packets on that node channel.

The process for packet based communication on the *HyperPlane* is described. Following these protocols, transmitted packets traverse the backplane over the optical node channels and are extracted via address recognition at the appropriate SPA for delivery to the user.

The protocol for a sending (n+1)-bit SPA node channel:

1. Packets are injected one word (n bits) at a time.
2. The first word (n bits) of each packet transmission consists of the packet header. This header contains the destination address of the accompanying packet data.
3. Idle data (the all zero string) is sent when no packet is available for transmission.

The protocol for a receiving (n+1)-bit SPA node channel:

1. Packets are extracted one word (n bits) at a time.
2. Packet extraction is initiated when: a) the address within a received packet header matches the corresponding SPA (user) fabric address, and b) the destination user is not busy.
3. Extraction ends after the entire packet is received.
4. At all other times, the SPA node channel is transparent.

3. SPA Implementation

A SPA for implementing a *HyperPlane* based ATM switch has been designed and fabricated using AT&T's CMOS-SEED technology[3]. The 2x4 SPA is comprised of 2 node channels of 4 smart pixels each. Each smart pixel contains 51 transistors (18 logic gates). The SPA and associated control logic totals 825 transistors in an area of approximately 500μm by 1250μm. Differential SEED pairs are used for optical input and output. The SEEDs used have 18μm active areas on a 125μm pitch. Figure 1 shows a photograph of the SPA along with a template of the circuit layout.

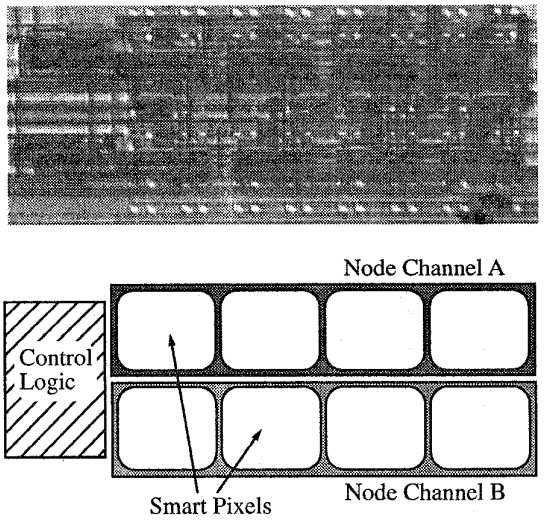

Figure 1. Photograph of SPA and layout template.

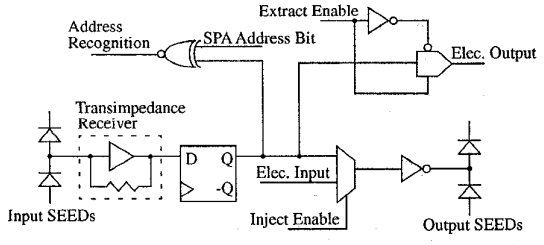

Figure 2. Smart Pixel Schematic.

4. Smart Pixel Circuit Topology

The smart pixel circuitry used in this design in shown in Figure 2. The smart pixel operation is synchronous, so that the optical input data is latched into the pixel by

a global system clock. Once latched, the bit can be operated on in several ways depending on the state of the smart pixel (or more generally, the node channel state). First, the address recognition circuitry, an XNOR gate, compares the data with the appropriate SPA address bit. The result of this comparison is used in conjunction with the address recognition results from other smart pixels in the node channel to validate packet headers and thus begin packet extraction. This validation and extraction setup is handled by the on-chip control logic. Second, once extraction has begun, extract enable will be set high and the optical input data will be extracted to the electrical output. Additionally, the input data will be optically regenerated at the output SEEDs when the smart pixel is in the transparent state. Finally, sending packet data (injection) from the electrical input is possible when inject enable is set high.

5. Transimpedance Optical Receiver

The transimpedance receiver stage used for the optical input is shown in Figure 3. The receiver was designed to operate at low input levels with minimal signal propagation delay. SPICE simulations indicate the propagation delay through the receiver to be less than 2.5ns with ±10μW of differential optical power at the input SEEDs. Additional SPICE characterization found the transimpedance gain (Z_T) to be 92 dB, the bandwidth ($f_{3\text{-dB}}$) to be 205 MHz, and the transimpedance-bandwidth product (TZBW) to be 60 Ω·GHz.

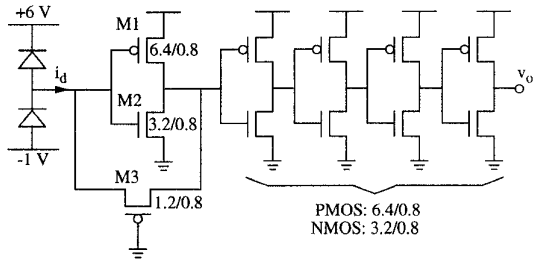

Figure 3. Transimpedance Receiver (W/L in μm).

6. Simulated SPA Performance

The full-custom layout of the chip was performed in Magic, and the subsequent layout extraction was simulated at both the circuit level in SPICE and at the switch level in IRSIM. Important digital delays to minimize for high speed operation include the transparent state delay (from the latch output Q to the output SEEDs) and the extraction delay (from the latch output Q to the electrical package pinout). These were found from IRSIM to be 0.6ns and 3.9ns, respectively. From these and other simulation values, the critical path was identified and was found to limit the system clock frequency to a maximum of 210 MHz. This is well in excess of the targeted system clock frequency of 155 MHz. In addition, the aggregate optical throughput of the SPA is found to be 1.24 Gbps (=155 Mbps per smart pixel * 8 smart pixels).

7. Measured SPA Performance

Electrical functional verification of the SPA was performed using copies of the CMOS-SEED chip which did not have SEEDs flip-chip bonded to their surface. The optical inputs of these chips were simulated by electrically probing onto the flip-chip bond pad sites. All of the functions of the SPA were verified as operating correctly, including: packet injection, address recognition, packet extraction, and transparency. Figure 4 is a photograph of the input and corresponding output trace of an individual smart pixel operating in transparency at 10 Mbps. Higher bit rates could not be demonstrated using this setup due to capacitive loading (>13pF) by the probe.

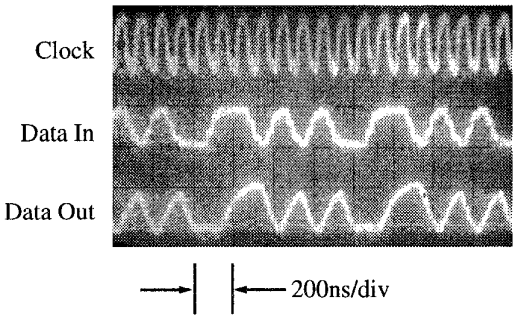

Figure 4. Smart Pixel Transparency.

Optical functional verification of the SPA was performed using a fully bonded version of the CMOS-SEED chip. Two independently adjustable optical beams at 850 nm were used to illuminate a differential SEED pair. Differential optical modulation at the smart pixel optical output was observed by clocking electrical data into the SPA, thus verifying smart pixel injection. Operation of the differential optical inputs and the transimpedance optical receiver at dc was also verified, at differential optical input powers as low as 12.5 μW.

8. Conclusion

Preliminary testing of a *HyperPlane* ATM based switch SPA has been successfully completed. Both the electrical and the optical functions of the chip have been verified. Future testing of this SPA will be focused on high speed verification in a chip-to-chip imaging setup.

9. References

[1]. T. H. Szymanski and H. S. Hinton, "Design of a Terabit Free-Space Photonic Backplane for Parallel Computing," *MPPOI'95,* San Antonio, TX, Oct. 23-24, 1995.

[2]. H. S. Hinton and T. H. Szymanski, "Intelligent Optical Backplanes," *MPPOI'95,* San Antonio, TX, Oct. 23-24, 1995.

[3]. K. W. Goossen et al, "GaAs MQW modulators integrated with silicon CMOS," IEEE Photonics Technology Letters, Vol. 7, 1995, pp. 360-362.