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Optical Backplane Demonstrators Based on FET-SEED Smart Pixel Arrays

by

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Abstract

We demonstrate a representative portion of an optical backplane using free-space optical channels to interconnect printed circuit boards which employ FET-SEED based smart pixel arrays. Results of system demonstrator performance will be presented.

Introduction

Free-space optical interconnects represent a solution to the needs of future connection-intensive digital systems such as ATM switching systems, and massively parallel processing computer systems. These systems will require the large board-to-board connectivity provided by an optical backplane created with two-dimensional arrays of passive, free-space, Parallel Optical Channels (POCs) to optically interconnect electronic Printed Circuit Boards (PCBs) and/or Multi-Chip Modules (MCMs). Such a backplane could be capable of supporting terabit/second aggregate capacities with connectivity levels on the order of 10,000 input/output channels per PCB.

FET-SEED Transmitter/Receiver circuits

We have developed the optics and optomechanics to demonstrate these high bit rate optical backplanes. As part of this program, we have constructed a representative portion of an optical backplane capable of interconnecting two printed circuit boards which utilize FET-SEED based smart pixel transceiver arrays.(1) Figure 1a shows a schematic of the transmitter circuit. At the input, the driver FET modulates the voltage across the Multiple Quantum Well (MQW) modulator pair resulting in differentially modulated output light. The electrical input impedance was designed for 50 ohms to ensure efficient coupling of high frequency signals to the optical modulator drive FET. Figure 1b shows a schematic of the receiver circuit. Here the high speed differential optical modulation is detected using a MQW diode pair. The diode pair output is fed to an inverting amplifier section of the circuit, and then further amplified using power FETs (375 μm gate width)

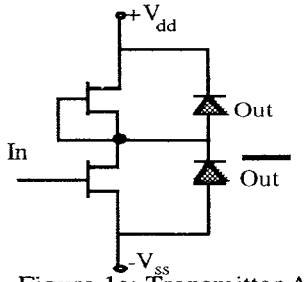

Figure 1a: Transmitter Array

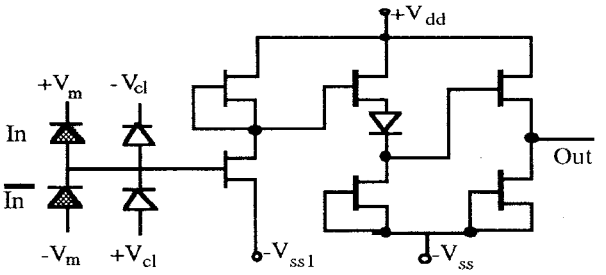

Figure 1b: Receiver Array

designed to drive 100 ohm transmission lines on a PCB. Both the 4 x 4 transmitter and receiver array optical windows are 25 x 25 μm, separated by 50μm, with the pixel to pixel pitch being set at 200μm.

Optical System Design

Board-to-board interconnection was accomplished using the two-sided optical backplane approach shown in Figure 2.[2] The optomechanics design was capable of implementing both a bulk optics approach, and a lenslet array based approach for creating the passive optical channels used to interconnect the PCBs. In both systems, light from the an argon laser pumped Ti:Sapphire laser is delivered and collimated using single mode fibers and collimating optics. A binary phase grating is used to provide spot array generation for illuminating the smart pixel array optical windows. Vertically polarized light is reflected off the polarization beam splitter, directed through a quarter waveplate, and focused onto the transmitter array. The transmitter circuit modulates the light, reflecting the light back towards the adjacent printed circuit board through the polarizing optics. The modulated light is detected by the receiver smart pixel photodiodes, and amplified using power FETs. These signals are then directed onto the PCB for appropriate processing. The optomechanics for this first demonstrator is based on a modified AT&T baseplate approach.[3] The baseplate is made from Magnesium to insure extreme flatness tolerances.

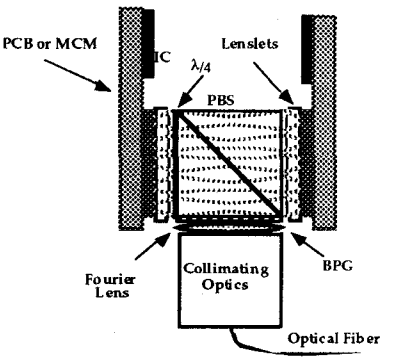

Figure 2: Demonstrator Schematic

Optical System Characterization

Figures 3a and 3b show eye diagrams of the system performance at 50 MBits/sec and 155 MBit/sec respectively. Additional system performance measurements and system characterization will be presented.

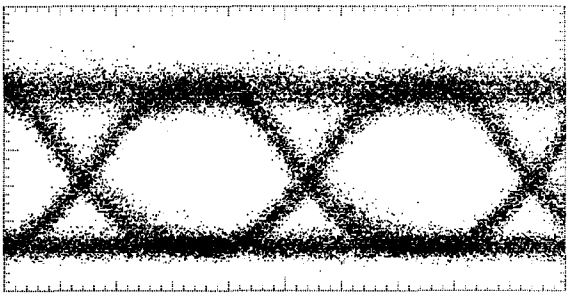
Figure 3a: 50 MBit/sec (5ns/div. and 20 mv/div.)

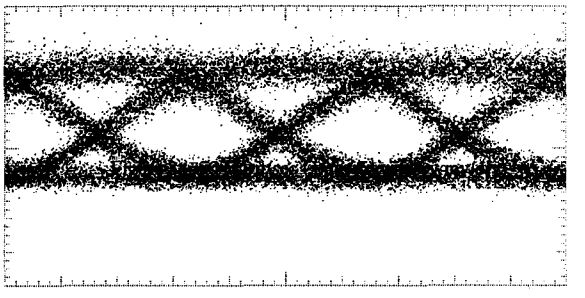
Figure 3b: 155MBit/sec (2 ns/div. and 15 mv/div.)

Acknowledgments

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3) F.B. McCormick et. al., Applied Optics, vol. 32, no. 26, pp. 5153-5171, 1993.