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FET-SEED Smart Pixel Layout Extraction and Simulation

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Summary

Smart pixels in conjunction with free-space optical interconnects permit the implementation of massively parallel and connection-intensive photonic system architectures. In general such architectures require complex processing functionalities for the smart pixel, such as ATM header processing, route multiplexing and digital transceiving. The implementation of such functionalities needs reasonably complex optoelectronic integrated circuits (OEIC). For example, a recently proposed hypermesh architecture [1] requires 26 transistors per pixel in an array that eventually will scale up to many thousands of pixels.

The design of these circuits can be eased with a design process or cycle supported by the proper computer-aided design (CAD) tools. The design process begins with a logic design and a circuit design to implement the desired functionality. The design is then laid out according to geometric design rules specific to a particular technology. Once the layout is completed, a battery of tests can be performed on the layout to verify whether or not the layout meets the design specifications. For example, we can directly check the layout for design rule inconsistencies with a design rule checker (DRC). However many design verifications and tests cannot be performed directly on the layout but necessitate an extraction. The extraction supplies a textual description or netlist of the circuit implemented by the layout. Only with a netlist, can an analog simulation of the layout be performed. The results of this simulation can then be used to validate the designed performance objectives.

In this paper, we discuss a segment of the design cycle for the FET-SEED technology and describe how two important CAD tools, namely an extractor and a simulator, were configured for the FET-SEED technology using L-EDIT™ and Microsim PSpice™. Although we used this physical layout editor (and its extractor) and the Microsim PSPICE™ simulator, the relevant points about extraction and simulation are not specific to either software packages. The discussion addresses general problems of extracting FET-SEED physical layouts and simulation of FET-SEED circuits.

Specifically, we designed and laid out a FET-SEED smart pixel receiver and transmitter circuits that were subsequently fabricated. We extracted the laid out circuits and performed an analog simulation on the extracted netlist. In order for the simulator to accurately predict the behavior of the fabricated chip, we correlated the simulation results with DC experimental measurements of our chip and configured the simulator for AC and time delay predictions.

Our approach to FET-SEED DC simulation is to use existing device models in the simulation of FET-SEED electronics (i.e. Field-Effect Transistors, PN-junction and Schottky diodes) and to use a table look-up method [2] for the FET-SEED optoelectronic devices (i.e. MQW diodes). We have found that existing models can predict FET-SEED electronics DC characteristics well. Figure 1 shows a fit between experimental current versus voltage characteristics (I-V curves) and modeled I-V curves for (a) a Schottky diode and (b) a FET. The FETs were modeled with the PSPICE based Raytheon model for GaAs FETs, and the diodes with a PSpice based diode model. In addition, the FET and diode internal capacitances were also modeled to reflect their respective device frequency characteristics.

AC circuit simulations of our smart pixel receiver and transmitter circuits show a 3 dB frequency cut-off of ~1.1Ghz (Fig.2) and ~7 Ghz (Fig.3), respectively. From transient simulations, we also found a delay of 3 ns and 0.5 ns for the receiver and the transmitter pixel,

respectively. These delays are consistent with theoretical predictions [3]. The correlation of these AC and transient simulations with experimental measurements will be presented.

We will present the configuration of an extractor and a simulator for the FET-SEED technology. These tools will be discussed in the context of the FET-SEED smart pixel circuits design cycle.

Acknowledgments

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References:

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3) A. L. Lentine, L. M. F. Chirovsky, and T. K. Woodward,"Optical Energy Considerations for simple Smart Pixel Receivers", submitted to IEEE J. Quantum Electronics, 1994.

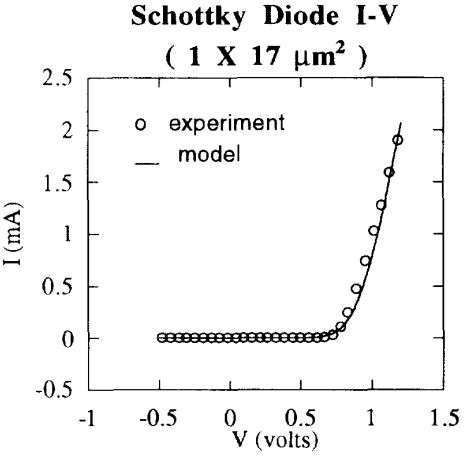

Fig.1a) Modeled Schottky diode (1 X 17 μm^2).

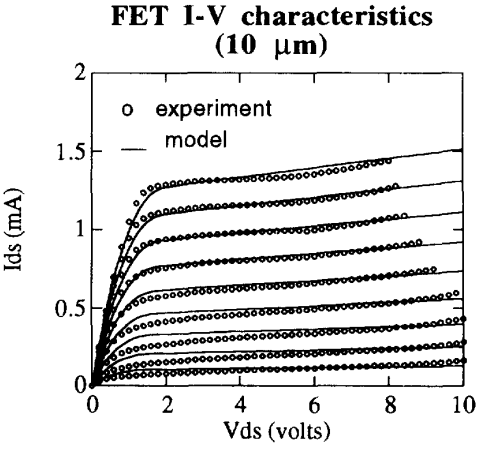

Fig. 1b) Modeled FET (10 μm wide) -1 V ≤ Vgs ≤ 0.6 V by 0.2 V step.

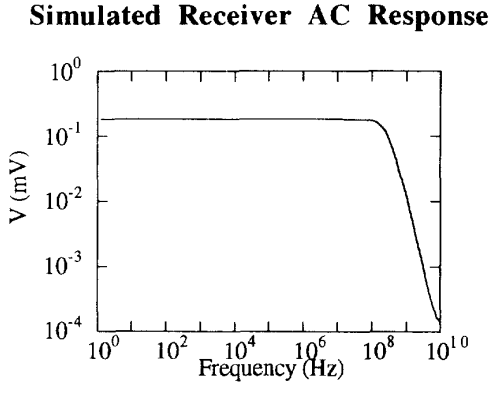

Fig.2: Receiver small signal frequency response (input amplitude = 10 μVolt).

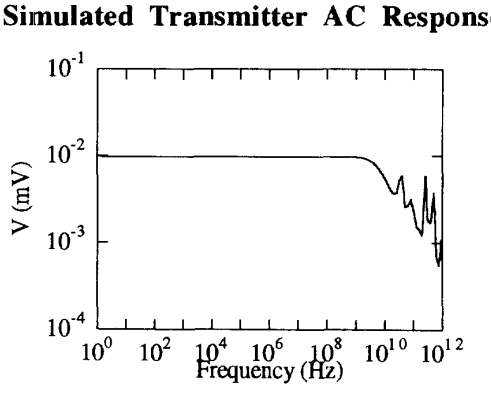

Fig.3: Transmitter small signal response (input amplitude = 10 μVolt).