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Design and Characterization of FET-SEED Smart Pixel Transceiver Arrays for Optical Backplanes

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Summary

Currently, we are developing the optical, optoelectronic, and optomechanical technology required to demonstrate a representative portion of a free-space optical backplane. Such a backplane can be created with two dimensional arrays of passive free-space Parallel Optical Channels (POCs) to optically interconnect the systems electronic Printed Circuit Boards and/or Multichip Modules (MCMs). Specific demonstration projects include the optical interconnection of PCBs via these passive optical channels using FET-SEED Smart Pixel transceivers. The first demonstrator will show the optical interconnection of a 4 x 4 FET-SEED transmitter array mounted on one PCB to an opposing 4 x 4 FET-SEED receiver array mounted on an adjacent PCB.

Based on these goals, FET-SEED based transmitter and receiver Smart Pixel circuits were designed and fabricated[1]. Figure 1a shows a schematic of the transmitter circuit. At the input, the driver FET modulates the voltage across the Multiple Quantum Well (MQW) modulator pair resulting in differentially modulated output light. The electrical input impedance was designed for 50 ohms to ensure efficient coupling of high frequency signals which will result in high speed operation of the optical modulators. Figure 1b shows a schematic of the receiver circuit. Here, the high speed optical modulation is detected using the MQW diode pair, fed to an amplifier section of the circuit, and then further amplified using power FETs (375 μm gate width) designed to drive 100 ohm transmission lines on a PCB. Both the 4 x 4 transmitter and receiver array optical windows are 25 x 25 μm, separated by 50μm, with the pixel to pixel pitch being set at 200μm.

In order to operate these transceivers at high frequencies (> 1 GBit/sec), the devices were mounted in a 68 pin, high-speed, multilayer ceramic package designed for 4 GBit/sec clock rates and edge speeds of less than 100 psec[2]. Here, the signals are carried on 50 Ohm controlled impedance transmission lines to the transmitter array or from the receiver array bond pads. This package is next mounted onto a PCB using a high speed, solderless connection capable of preserving the 4 GHz bandwidth of the 68-pin package. The PCB output is through standard 50 ohm coaxial connectors to insure a clean interface to both the PCB transmission lines, and the package signal lines.

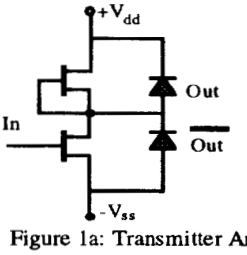

Figure 1a: Transmitter Array

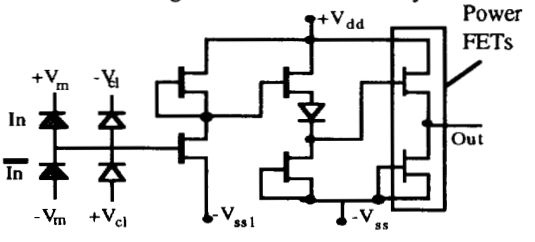

Figure 1b: Receiver Array

Preliminary measurements of the FETs,

Schottky diodes, MQW diodes, and the transceiver circuits were performed. In addition, the functionality of the fabricated circuits was verified. Figures 2a and 2b show typical I-V curves of a Schottky diode and a FET, respectively on the fabricated chips (experimental and modeled). The optical modulators were measured and showed a reflectivity change of 3 to 1 with -7.5 volts of applied bias. The optical modulator pair in the transmitter circuit exhibited a 2 to 1 ratio in reflectivity when measured at low frequencies. The transmitter circuit was characterized to 2 MBits/sec and exhibited no degradation in performance. The receiver circuit was characterized to 4 KBits/sec and also showed no degradation in performance. AC simulations of the smart pixel receiver and transmitter circuits show a 3 dB cut off frequency of 1.1 GHz and 7 GHz respectively. High speed measurements of device and circuit performance, followed by correlation to SPICE™ modeling currently underway will be presented[3].

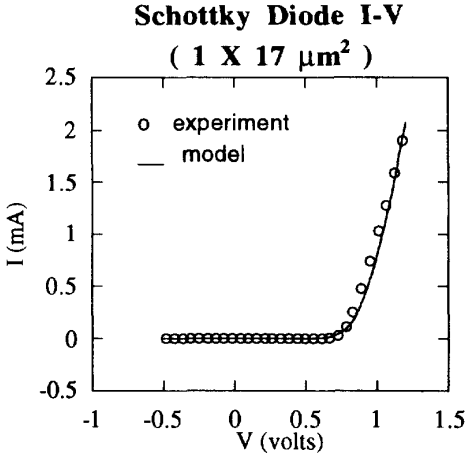

Fig.2a) Schottky diode.

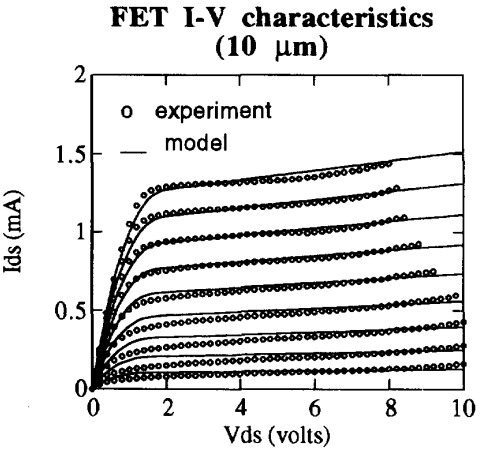

Fig. 2b) FET (-1V≤Vgs ≤0.6V by 0.2V)

Finally, performance of the FET-SEED transceiver circuits in a representative portion of an optical backplane using free-space optical channels to interconnect the PCBs will be presented. Results of a 4x4 interconnection will be described, and the performance of these smart pixel circuits will be discussed. In addition, the capabilities of this technology when implemented in board-to-board optical interconnection systems will be described.

Acknowledgments

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