Experimental Study of Burst-Mode Reception in a 1300 km Deployed Fiber Link

Bhavin J. Shastri, Yousra Ben M'Sallem, Nicholas Zicha, Leslie A. Rusch, Sophie LaRochelle, and David V. Plant

Abstract—We experimentally demonstrate burst-mode reception in a 1300 km fiber link that spans from Montreal to Quebec City and back, with a 1.25 Gb/s burst-mode receiver (BMRx). The receiver features automatic phase acquisition using a clock phase aligner (CPA) and provides instantaneous (0 preamble bit) phase acquisition with error-free operation [packet-loss ratio (PLR) $<10^{-6}$ and bit error rate (BER) $<10^{-10}$] for any phase step ($\pm 2\pi$ rad) between consecutive packets, while also supporting more than 1100 consecutive identical digits (CIDs). The CPA makes use of a phase picking algorithm and an oversampling semi-blind clock and data recovery circuit operated at $2\times$ the bit rate. We also study the effect of channel impairments on the performance of BMRx at such distances. More specifically, we investigate the PLR performance of the system and quantify it as a function of the phase step between consecutive packets, received signal power, CID immunity, and BER, while assessing the trade-offs in preamble length, power penalty, and pattern correlator error resistance.

Index Terms—Burst-mode receiver; Clock and data recovery (CDR); Clock phase aligner (CPA); Optical fiber communications; Optical networks.

I. INTRODUCTION

Large-scale computer networks are needed to support growing web applications that require fast and reliable interconnections to provide rapid access to information and services to millions of users. As the number of interconnected servers and storage media increases, optical technologies are expected to play a major role in the development of these local area networks (LANs) because of the high speed, low loss, and small foot print of optical fiber communication links. Optical packet switched networks (OPSNs) are expected to overcome future bottlenecks in transport and access networks as they reduce the number of layers present in the current protocol stack to only two levels: Internet protocol (IP) over optical.

Much research into OPSNs focuses on the optical design, while assuming the availability of high-speed electronics [1–4]. Also, the effect of channel impairments on the performance of electronic receivers has largely been overlooked. For example, silence periods between packets are inevitable and inherently arise in OPSNs due to the statistical multiplexing. In fact, the sent packets only occupy capacity in the network when there is data to be routed over the network, whereas in silent periods the capacity becomes available to other traffic streams [5]. This asynchronous nature of silence periods can cause conventional receivers, clock and data recovery (CDR) circuits based on phase-locked loops (PLLs), to lose pattern synchronization. Preamble bits can be inserted at the beginning of each packet to allow the CDRs enough time to acquire lock. However, this overhead reduces the effective throughput and increases delay.

In this paper, we implement an electronic receiver that features postprocessing functionalities, a burst-mode receiver (BMRx), with applications to OPSNs in long-distance networks. This BMRx is comprised of a semi-blind oversampling CDR circuit operated at $2\times$ the bit rate and a clock phase aligner (CPA) that makes use of a phase picking algorithm for automatic clock phase acquisition. The most important characteristic of the CPA is its phase acquisition time, which must be as short as possible to decrease the burst-mode sensitivity penalty and thus increase the power budget or alternatively increase the information rate
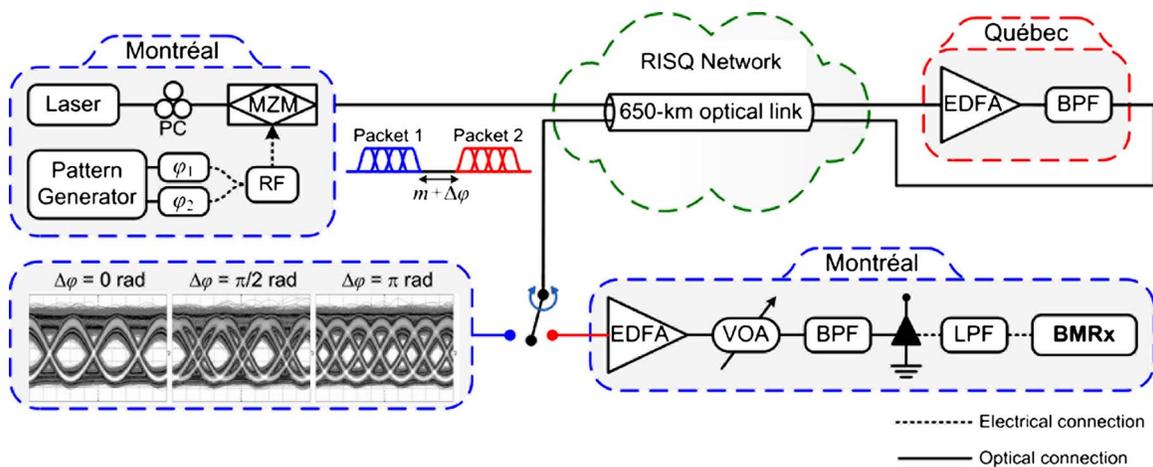
Fig. 1.   (Color online) Experimental setup for burst-mode reception in the 1300 km deployed fiber link. (PC, polarizer controller; RF, radio-frequency power combiner; MZM, Mach–Zehnder modulator; EDFA, erbium-doped fiber amplifier; BPF, bandpass filter; VOA, variable optical attenuator; LPF, low-pass filter; BMRx, burst-mode receiver). Details of the packet structure and the BMRx are depicted in Fig. 2 and Fig. 4, respectively.

with more bits available to the packet payload. The strength of our approach is the exploitation of components designed to operate at high bit rates in support of transport network bit rates. The proposed BMRx architecture could in principle be scaled up to 10 Gb/s and even to 40 Gb/s. Such high-speed receivers with rapid data recovery time are required for future optical switched networks.

We demonstrate experimentally for the first time, to our knowledge, burst-mode reception in a 1300 km deployed fiber link that spans from Montreal to Quebec City and back, over a RISQ[1] network. We investigate the effects of channel impairments on the performance of BMRx in terms of the packet-loss ratio (PLR) and bit error rate (BER) and quantify it as a function of the phase step between consecutive packets, received signal power, and CID immunity. We also assess the trade-offs in preamble length, power penalty, and pattern correlator error resistance. These results will help refine theoretical models of receivers employed in the OPSN and provide input for establishing realistic power budgets.

The rest of the paper is organized as follows: In Section II, we present the experimental setup, describe the design and implementation of the BMRx, and explain in detail the deployed 1300 km fiber link. Section III is devoted to the presentation and analysis of the experimental results. Finally, the paper is summarized and concluded in Section IV.

II. EXPERIMENTAL SETUP, RISQ NETWORK, AND BURST-MODE RECEIVER CONFIGURATION

A. Experimental Setup

The experimental setup illustrated in Fig. 1 is used

[1]Réseau d'informations scientifiques du Québec (Quebec's Scientific Information Network), www.risq.qc.ca.

to test the 1300 km deployed fiber link. A distributed-feedback (DFB) laser at 1538.98 nm is modulated by 1.25 Gb/s bursty data. Bursty traffic is generated by adjusting the phase φ_1 and φ_2 between alternating packets from two programmable ports of an Anritsu MP18000 pattern generator, which are then concatenated via a radio-frequency (RF) power combiner and used to drive a polarization-dependent Mach–Zehnder modulator (MZM) with an optical modulator driver also from JDSU (model #H301-1110).

The time between two consecutive packets corresponding to the laser ON/OFF time is 16 bits. As depicted in Fig. 2, the packets are formed from 0 to 48 (l) preamble bits, 36 delimiter bits, $2^{15}-1$ payload bits, and 48 comma bits. The preamble bits are used to perform phase recovery. The delimiter is a unique pattern indicating the start of the packet and exploited for byte synchronization. Similarly, the comma is a unique pattern to indicate the end of the payload. The payload is simply a $2^{15}-1$ pseudorandom binary sequence (PRBS). The PLR and BER measurements are only performed on the delimiter and payload bits, respectively.

The lock acquisition time corresponds to the number of bits (l) needed in front of the delimiter in order
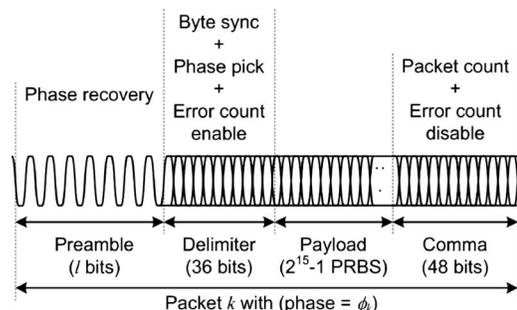
Fig. 2.   Packet structure for the experiment.

to achieve error-free operation, that is, PLR $<10^{-6}$ and BER $<10^{-10}$, for any phase step, $|\Delta\varphi| = |\varphi_1 - \varphi_2| \leqslant 2\pi$ rad, between any two consecutive packets in the link. Note that this method of measuring the phase acquisition time is more accurate than the qualitative method of monitoring the CDR's voltage-controlled oscillator (VCO) control voltage [6]. In the latter case, the phase acquisition time is determined by measuring the settling time of the VCO's control voltage envelope to within a certain percentage of the steady-state value. The drawback of this method is that it overestimates the lock acquisition time as it is not necessary for the clock to be perfectly aligned with the data before the payload becomes valid.

A silence period T_S (guard time), consisting of a phase step $|\Delta\varphi|$ (with a 1 ps resolution), and an all-zero sequence of m consecutive identical digits (CIDs) can be inserted between the packets. The silence period can be expressed as

$$T_s = \left(m + \frac{\Delta\varphi}{2\pi} \right) T, \qquad (1)$$

where T is the bit period. The phase steps between the consecutive packets can be set anywhere between ± 1 ns on a 1 ps resolution, corresponding to a ± 1.25 unit interval (UI) at 1.25 Gb/s. Note that 1 UI corresponds to a 1 bit period. Eye diagrams of the bursty traffic input to the BMRx are shown in Fig. 1 with different phase steps: $\Delta\varphi = 0$ rad (0 ps), $\Delta\varphi = \pi/2$ rad (200 ps), and $\Delta\varphi = \pi$ rad (400 ps).

The bursty data is then sent over the RISQ network on a link consisting of 650 km of standard single-mode fiber (G.652) link from Montreal to Quebec City, as seen in Fig. 1. At Quebec City, the signal is amplified by an erbium-doped fiber amplifier (EDFA) and band-pass filtered (BPF) before being looped back. In Montreal, the signal undergoes amplification by an EDFA before a variable optical attenuator (VOA) serves to control the received power level. The signal is then filtered before the optical-to-electrical conversion is performed by a PIN photodiode from New Focus (model #1434). The bursty signal is then low-pass filtered (LPF) before being sent to the BMRx. The LPF is a fourth-order Bessel–Thomson filter whose −3 dB cutoff frequency is $0.7\times$ the bit rate, or 875 MHz, to remove the out-of-band high-frequency electrical noise. Such a filter has an optimum bandwidth to filter out noise while keeping intersymbol interference (ISI) to a minimum [7].

B. RISQ Network

RISQ refers to both the network and the organization that manages the high-speed optical access network that supports research and higher-education institutions throughout Quebec with sophisticated telecommunications services. The RISQ network is the Quebec portal for the Canada-wide network (CA*net). We used an unoccupied wavelength on the wavelength-division-multiplexed RISQ network to measure the effect of real-world channel impairments on our BMRx at 1.25 Gb/s. There are ten amplification stages featuring both EDFAs and dispersion compensation modules on the 650 km fiber link from Montreal to Quebec City. Considering the extra amplifier at the loop-back point, this implies a total of 21 amplification stages on the 1300 km deployed link.

We measured the residual chromatic dispersion of the link using the phase-shift method ($f_{mod} = 100$ MHz, Anritsu model 8509BR). The group delay measurement, shown in Fig. 3, is performed with 16 averages and fitted to the standard linear polynomial. We consider only the first-order dispersion because we realize our experiments at a bit rate that is less than 10 Gb/s and over a narrow waveband (0.2 nm). The residual chromatic dispersion thus obtained is 2533.25 ps/nm over the channel bandwidth. This residual dispersion is not expected to have any significant impact on 1.25 Gb/s transmission.

C. Burst-Mode Receiver Configuration

The main building blocks of the receiver are illustrated in Fig. 4. Our BMRx without the double-data rate (DDR) functionality is similar to the 622 Mb/s receiver in [8]. The receiver includes a multirate synchronous optical network (SONET) CDR from Analog Devices (part #ADN2819), a 1:16 deserializer (DES) from Maxim-IC (part #MAX3885), and a CPA module implemented on a Virtex IV field-programmable gate array (FPGA) from Xilinx. The multirate CDR recovers the clock and data from the incoming signal. The CDR supports the following frequencies of interest: 1.25 and 2.5 Gb/s for burst-mode operation at $2\times$ the bit rate. The CDR is followed by a 1:16 deserializer
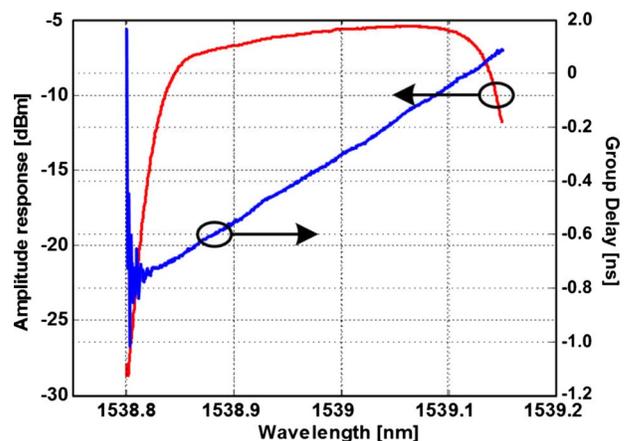
Fig. 3. (Color online) Measured residual dispersion in a loop-back (Montreal–Quebec City) of RISQ link.
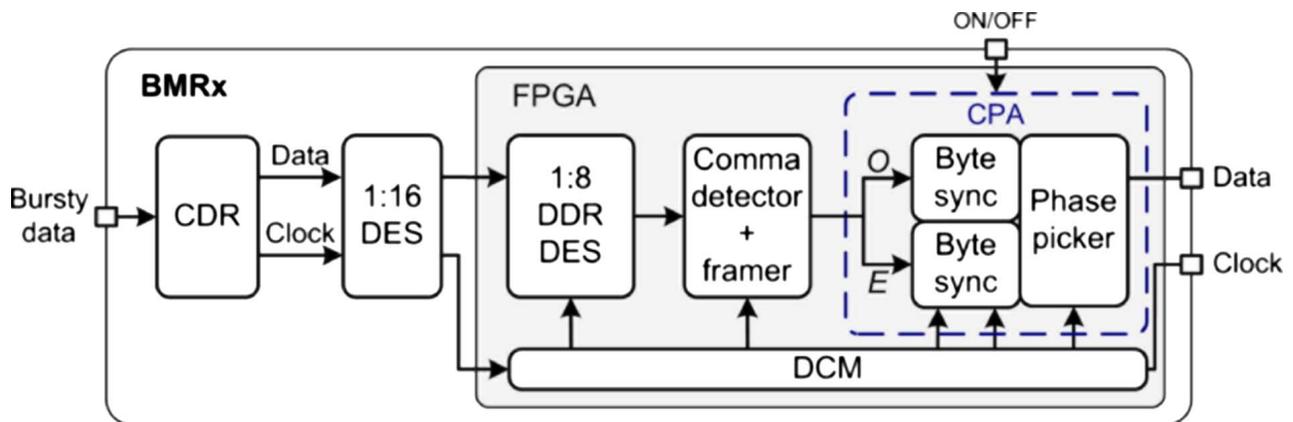
Fig. 4.   (Color online) Block diagram of the burst-mode receiver (CDR, clock and data recovery; DES, deserializer; DDR, double-data rate; CPA, clock phase aligner; DCM, digital clock manager; Sync, synchronizer).

that reduces the frequency of the recovered clock and data to a frequency that can be processed by the digital logic. The lower rate parallel data is then sent to the FPGA for further processing. Thereafter, a 1:8 DDR DES, a framer, a comma detector, the CPA (including byte synchronizers and a phase picker), and a digital clock manager (DCM) are implemented on the FPGA. Note that our CPA is designed to support data rates up to 5 Gb/s with 10 Gb/s sampling rates. However, due to unavailability of commercial multirate CDRs at 5 Gb/s, at the time of writing this paper, the BMRx was instead tested at 1.25 Gb/s with 2.5 Gb/s sampling rates.

On the board it is first necessary to further parallelize the data and clock to a lower frequency that will ensure proper synchronization and better stability of the DCM before these signals can be sent to the CPA for automatic phase acquisition. Thus, an integrated DDR 1:8 DES is implemented on the FPGA. Automatic detection of the payload is implemented on the FPGA through a framer and a comma detector, which are responsible for detecting the beginning (delimiter bits) and the end (comma bits) of the packet, respectively. The CPA makes use of a phase picking algorithm and the $2\times$ oversampling CDR. The CPA is turned ON for the PLR measurements with phase acquisition for burst-mode reception when $\Delta\varphi \neq 0$ rad; otherwise it can be bypassed for continuous-mode reception when $\Delta\varphi = 0$ rad.

The idea behind the CPA is based on a simple, fast, and effective algorithm. The odd and the even samples resulting from sampling the data twice on the alternate (odd and even) clock rising edges are forwarded to path O and to path E, respectively. The byte synchronizer is responsible for detecting the delimiter. It makes use of a payload detection algorithm to look for a preprogrammed delimiter pattern. The concept behind the phase picking algorithm is to replicate the byte synchronizer twice in an attempt to detect the de-

limiter on either the odd and/or even samples of the data, respectively. That is, regardless of any phase step, $|\Delta\varphi| \leqslant 2\pi$ rad, between two consecutive packets, there will be at least one clock (odd or even) edge that will yield an accurate sample. The phase picker then uses feedback from the byte synchronizers to select the right path from the two possibilities. The realigned data is then sent to a BER/PLR tester.

III. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 5(a) shows the PLR performance of the 1300 km fiber link as a function of phase difference $\Delta\varphi$ between consecutive packets for different preamble lengths with only the CDR (CPA turned OFF). The received signal power is kept at −18 dBm. We consider that all packets are correctly received when PLR $<10^{-6}$, corresponding to a BER $<10^{-10}$. We have restricted the horizontal axis to values of $0 \leqslant \Delta\varphi \leqslant 800$ ps, corresponding to $0 \leqslant \Delta\varphi \leqslant 2\pi$ rad at 1.25 Gb/s. Also, note that the results are symmetrical about 0 rad from $-2\pi \leqslant \Delta\varphi \leqslant 0$ rad. We observe a bell-shaped curve centered at 400 ps because this represents the half bit period corresponding to the worst-case phase step at $\Delta\varphi = \pi$ rad, and therefore, the CDR is sampling exactly at the edge of the data eye, resulting in a PLR ~1. At relatively small phase shifts (near 0 or 2π rad), we can easily achieve zero PLR because the CDR is almost sampling at the middle of each bit. Preamble bits ("1010 ···" pattern) can be inserted at the beginning of the packets to help the CDR settle down and acquire lock. As the preamble length is increased, there is an improvement in the PLR. At least 49 preamble bits are required for error-free operation for any phase step. However, the use of the preamble reduces the effective throughput and increases delay. By switching ON the burst-mode functionality of the receiver with the CPA as shown in Fig. 5(b), we observe error-free operation for any phase step with no
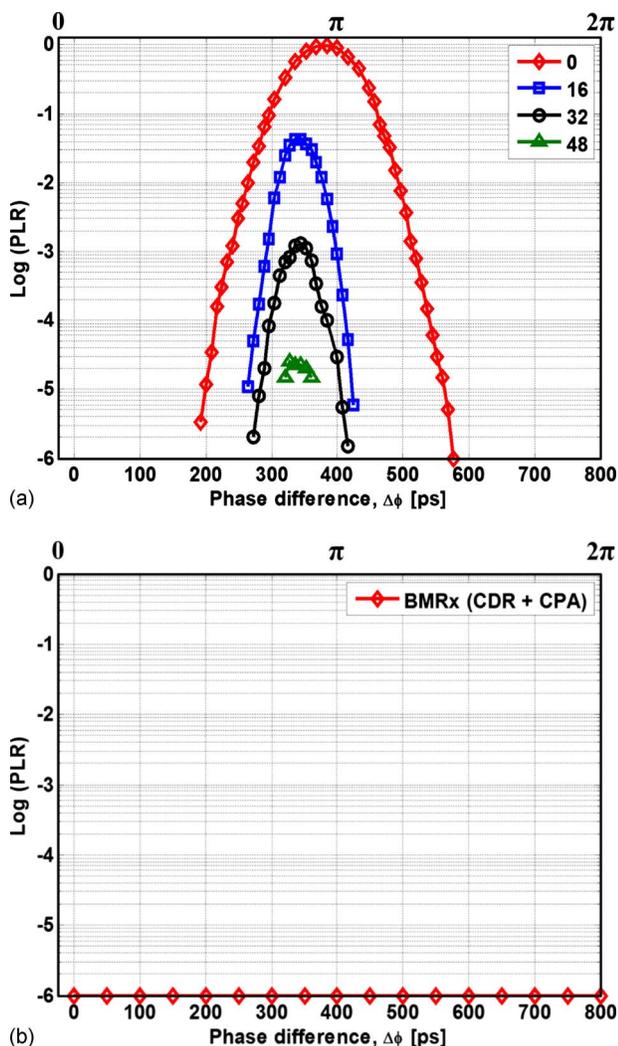
Fig. 5.   (Color online) PLR versus phase difference between consecutive packets. (a) CDR performance with different preamble lengths. (b) BMRx performance with no preamble bits.

Fig. 6.   (Color online) BER and PLR versus received signal power for different preamble lengths and phase steps between consecutive packets.

preamble bits, allowing for instantaneous phase acquisition. It should be noted that, whereas $\Delta\varphi = \pi$ rad represents the worst-case phase step for the CDR sampling at the bit rate, the $\Delta\varphi = \pi/2$ rad phase step is the worst-case scenario for the BMRx as it is based on an oversampling CDR at $2\times$ the bit rate.

We note that a sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet [9]. However, by reducing the phase acquisition time as demonstrated in this work, the burst-mode sensitivity penalty can be reduced. Alternatively, with the reduced number of preamble bits, more bits can be left for the payload, thereby increasing the information rate. To further illustrate this, consider the experimental results in Fig. 6, which shows the BER and PLR performance of the receiver as a function of the received signal power for different phase steps and preamble lengths. Note that the abscissa is the received signal power, that is, the optical power contributed at the photodiode. To determine the burst-mode penalty of the receiver, the performance of the CDR sampling continuous data ($\Delta\varphi = 0$ rad) at the bit rate is compared with the performance of the BMRx sampling bursty data with a worst-case phase step ($\Delta\varphi = \pi/2$ rad) as shown in Fig. 6(a). Both measurements are made for a 0 bit preamble. Due to the $2\times$ oversampling (faster electronics) and the phase picking algorithm, we observe a 2 dB and a 0.5 dB power penalty for the BER and PLR performance, respectively. It can also be observed that for the worst-case phase step in the link, the BMRx accomplishes sensitivities of −23 and −19.5 dBm, to achieve BER $= 10^{-10}$ and PLR $= 10^{-6}$, respectively. Note that when the BMRx samples continuous data, we actually notice a 1 dB improvement in the PLR performance over the CDR due to the CPA as depicted in Fig. 6(b). The CDR will not be able to recover any packets if there exists a worst-case phase step ($\Delta\varphi = \pi$ rad) between the consecutive packets, regardless of the received signal power, resulting in a PLR ∼1. However, if a 48 bit

preamble is complied with, the PLR performance of the CDR is then comparable with the PLR performance obtained by the CDR with zero preamble bits and no phase steps. Hence, for the worst-case phase steps in the link, there is a trade-off between the sensitivity penalty obtained by employing the BMRx over the CDR and the number of preamble bits required without the BMRx. Since random silence periods in a live link are inevitable, the power penalty may be a small price to achieve error-free operation.

We measure the CID immunity of the receiver by zeroing bits at the end of packet 1 until error-free operation can no longer be maintained on packet 2. The immunity of the BMRx and the CDR to CIDs is depicted in Fig. 7. The received signal power is kept at −18 dBm, with the phase step and the preamble length both set to zero for this measurement. As shown, both the BMRx and the CDR can support ~1100 CIDs with error-free operation. This CID immunity is significantly greater than current state-of-the-art BMRx—32 bits in [10] and 7 bits in [11]. It should be noted that in addition to CIDs, if a worst-case phase step is introduced between consecutive packets, the CDR regardless of its CID immunity will result in a PLR ~1. This is not the case with the BMRx, which as demonstrated, is immune to any phase steps between consecutive packets.

Finally, to measure the dynamic range of the receiver, we fix the amplitude of packet 1 and increase or decrease the amplitude of packet 2 until the BMRx can no longer maintain error-free operation on packet 2. Again, the phase step and the preamble length are both set to zero for this measurement. The worst-case scenario is when a low-amplitude packet follows a high-amplitude packet [12]. The dynamic range of the receiver is measured to be 3 dB. This relaxes the requirements of the output voltage swings/fluctuations
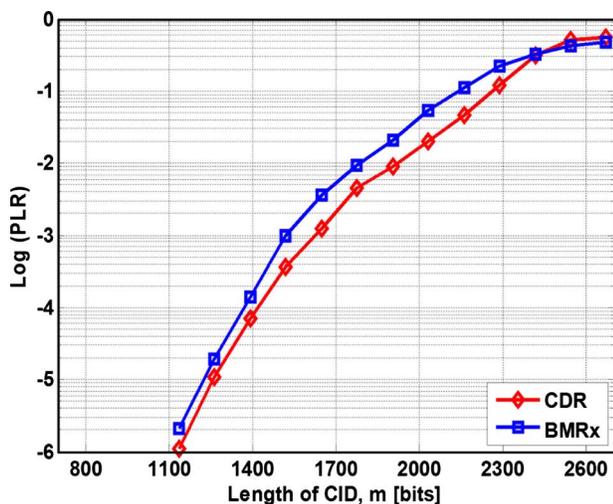
Fig. 7.   (Color online) PLR versus CID immunity of CDR and BMRx.

from a front end at high data rates. The dynamic range can easily be increased to more than 15 dB with a front end consisting of a burst-mode amplitude recovery circuit [13].

We now theoretically derive an expression that relates the PLR performance of the receiver as a function of the signal-to-noise ratio (SNR). The SNR will affect the bits in the packet delimiter. If the delimiter is not being correctly detected, a packet is declared lost, hence contributing to the packet loss count. The Q factor is the SNR at the decision circuit in voltage, and can be expressed as

$$Q = \frac{\mu_1 - \mu_0}{\sigma_1 + \sigma_0}, \tag{2}$$

where $\mu_{1,0}$ are the mean voltage values for the bits "1" and "0", respectively, while $\sigma_{1,0}$ are the corresponding standard deviations. The resulting BER denoted as P_e, can be determined by

$$P_e = \frac{1}{2} \operatorname{erfc}\left(\frac{Q}{\sqrt{2}}\right), \tag{3}$$

where

$$\operatorname{erfc}(x) = P_e = \frac{2}{\sqrt{\pi}} \int_x^\infty \exp(-\lambda^2) \mathrm{d}\lambda. \tag{4}$$

The error resistance [14] of the delimiter depends not only on its length, but also on the exact implementation of the pattern correlator. Let P_l^z represent the PLR obtained at a given signal power with a pattern correlator having an error resistance of z bits in a d bit delimiter. The PLR, P_l^z, can then be estimated as

$$P_l^z \leqslant \sum_{j=z+1}^{d} P(j) \approx P(z+1) \text{ for } P_e \ll 1, \tag{5}$$

where $P(x)$ gives the probability of finding x errors out of a d bit delimiter given that the probability of finding a bit error is P_e, and can be expressed as a binomial distribution:

$$P(x) = \frac{d!}{x!(d-x)!} P_e^x (1 - P_e)^{d-x}. \tag{6}$$

Using Eqs. (2)–(6), we theoretically predict the PLR performance P_l^z of the RISQ network as a function of the received signal power, with a pattern correlator having an error resistance of $z = 0$ bits, and compare the results experimentally in Fig. 8(a); the theoretical and experimental results concur.

To improve the system performance, forward-error-correcting (FEC) schemes can be employed by encoding the packet bits. Due to the associated overhead, most standards impose a strict requirement on the delimiter field—a unique pattern of fixed length. There-
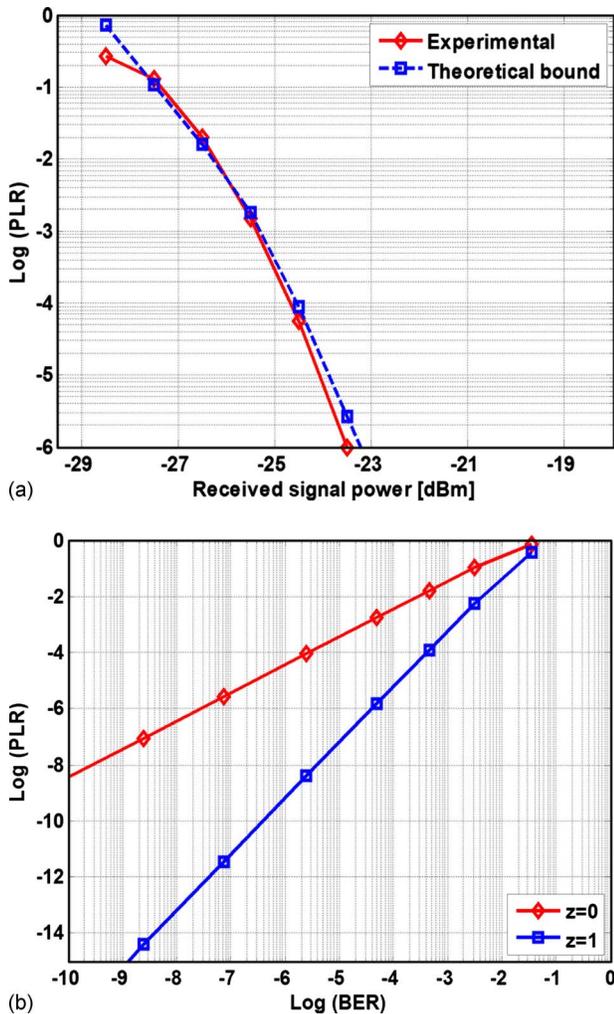
Fig. 8.   (Color online) (a) Comparison between theoretical and measured PLR versus signal power. (b) PLR versus BER performance with a pattern correlator having different error resistance values in the delimiter.

fore, while the payload bits can be encoded, it is usually not possible to encode the delimiter bits. Hence, while there is an improvement in the BER performance at a given SNR, the same cannot be implied about the PLR performance, which is dependent on the delimiter being correctly identified. Consequently, the BER may not be a true reflection of the system performance, but that of the properly received bursts only, as many other bursts may be lost without being included in the BER measurement.

The PLR performance can be improved by increasing the error resistance of the pattern correlator with a more sophisticated design of the pattern correlator. Thus, the complexity of the pattern correlator depends on an acceptable error resistance of the delimiter. Consider Fig. 8(b) where we plot Eq. (5), that is, the PLR performance P_l^z, as a function of the BER P_e, for different error-resistance values z, of the delimiter. Even with a simple pattern correlator having no error

resistance ($z=0$ bits), we obtain error-free operation: $PLR < 10^{-9}$ at $BER = 10^{-10}$. Furthermore, by increasing the pattern correlator error resistance to $z=1$ bit, we obtain an improvement in the PLR performance by eight orders of magnitude.

IV. CONCLUSION

We have experimentally investigated the effect of real-world channel impairments on the performance of a BMRx at 1.25 Gb/s in a 1300 km fiber link that spans from Montreal to Quebec City and back and quantified the results in terms of the BER and PLR performance of the system. The receiver features a semi-blind oversampling CDR circuit operated at $2\times$ the bit rate and a CPA with a phase picking algorithm for automatic clock phase acquisition.

The receiver achieves a $PLR < 10^{-6}$ and BER $< 10^{-10}$ while featuring instantaneous (0 preamble bit) phase acquisition for any phase step ($\pm 2\pi$ rad) between packets, a sensitivity of −19 dBm, a CID immunity of 1100 bits, and a 3 dB dynamic range. The price to pay is faster electronics and a burst-mode penalty of 2 and 0.5 dB in the BER and PLR performance, respectively. On the other hand, the 1.25 Gb/s BMRx inherits the low-jitter transfer bandwidth (2 MHz) and the low jitter-peaking (0.1 dB) of the oversampling CDR at 2.5 Gb/s. Hence, this receiver could also find applications in future OPSNs, which may require a cascade of BMRx that each consumes some of the overall jitter budget of the system.

Our solution leverages the design of components for long-haul transport networks using low-complexity, commercial electronics providing a cost-effective solution for OPSN receivers. These components are typically a generation ahead of the components for multi-access networks. Thus, our solution will scale with the scaling for long-haul networks, and will provide a simple way to evaluate the performance and quality of service of future OPSNs.

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Bhavin J. Shastri was born in Nairobi, Kenya, in 1981. He received Honors B.Eng. (with distinction) and M.Eng. degrees in electrical and software engineering from McGill University, Montreal, QC, Canada, in 2005 and 2007, respectively. He is currently working toward his Ph.D. degree in electrical engineering at the Photonic Systems Group of McGill University. His research interests include high-speed burst-mode optical receivers, clock and data recovery circuits, optoelectronic-VLSI systems, image processing, and computer vision. Mr. Shastri is the recipient of the prestigious Alexander Graham Bell Canada Graduate Scholarship (2008) from the National Sciences and Engineering Research Council of Canada (NSERC). He is a Lorne Trottier Engineering Graduate Fellow, and the recipient of the McGill Engineering Doctoral Award (2007). He is the co-recipient of the Silver Leaf Certificate for the Best Student Paper at the IEEE Microelectronics and Nanoelectronics Research Conference (2008). He won the Center for Advanced Systems and Technologies in Communications (SYTACom) Student Research Competition (2009), two Best Student Poster Awards at the Canadian Institute for Photonic Innovation (CIPI) Annual Workshop (2007, 2008), and was awarded the IEEE Laser and Electro-Optics Society (LEOS) Travel Grant (2007). He is also the recipient of the IEEE Computer Society Lance Stafford Larson Outstanding Student Award (2004), the IEEE Canada Life Member Award for the Best Student Paper (2003), the James McGill Award (2005), and the Faculty of Engineering Award (2001) for being ranked in the top 5%. He is a student member of the IEEE Photonics Society and the Optical Society of America (OSA) and the current Vice-President of the McGill OSA Student Chapter.

Yousra Ben M'Sallem was born in Tunisia in 1982. She received her telecommunications engineer diploma in June 2006 at SUP'COM (Ecole Supérieure des Communications de Tunis). She received her M.Eng. degree in electrical engineering from Laval University in 2008. In September 2008, she started a Ph.D. thesis on the future optical packet switched networks supervised by Professor Leslie A. Rusch. She is a student member of the IEEE Photonics Society. She is the recipient of the FQRNT International Internship Program for 2010.

Nicholas Zicha was born in Montreal, Canada, in 1981. He received his Honors B.Eng. (with distinction) in electrical engineering from McGill University, Montreal, Canada, in 2004. After working in industry as a digital hardware designer, he is currently pursuing his M.Eng. degree in electrical engineering at McGill University. His research interests include high-speed burst-mode optical receivers, high-speed interchip communications, and optoelectronic-VLSI systems.

Leslie A. Rusch received her B.S.E.E. (honors) degree from the California Institute of Technology, Pasadena, in 1980 and her M.A. and Ph.D. degrees in electrical engineering from Princeton University, Princeton, NJ, in 1992 and 1994, respectively. She was manager of a group researching new wireless technologies at Intel Corporation from 2001 to 2002. Currently, she is a Full Professor in the Department of Electrical and Computer Engineering at Université Laval, Québec, QC, Canada, performing research in wireless and optical communications. Her research interests include optical-code-division multiple access and spectrum-sliced WDM using incoherent sources for passive optical networks; semiconductor and erbium-doped optical amplifiers and their dynamics; radio-over-fiber; and in wireless communications, high-performance and reduced-complexity receivers for ultrawideband systems employing optical processing. Dr. Rusch is a member of the Optical Society of America, the IEEE Lasers and Electro-Optics Society, and the IEEE Communications Society.

Sophie LaRochelle received her B.Eng. degree in engineering physics from Université Laval, Sainte-Foy, QC, Canada, in 1987 and her Ph.D. degree in optics from the University of Arizona, Tucson, in 1992. From 1992 to 1996, she was a Research Scientist at the Defense Research and Development Canada-Valcartier, where she worked on electro-optical systems. She is currently a Professor at the Department of Electrical and Computer Engineering, Université Laval, where she holds a Canada Research Chair in Optical Fibre Communications and Components. She is a member of the Center for Optics, Photonics and Laser. Her current research activities are focused on active and passive fiber optics components for optical communication systems, including fiber Bragg gratings, optical amplifiers, and multiwavelength and pulsed fiber lasers. Her other research interests include packet-switched networks with photonic code processing, transmission of radio-over-fiber signals, and optical code-division multiple access. Dr. LaRochelle is a member of the Optical Society of America and the IEEE Lasers and Electro-Optics Society.

David V. Plant received his Ph.D. degree in electrical engineering from Brown University, Providence, RI, in 1989. From 1989 to 1993, he was a Research Engineer at the Department of Electrical and Computer Engineering, University of California at Los Angeles (UCLA). He has been a Professor and Member of the Photonic Systems Group, the Department of Electrical and Computer Engineering, McGill University, Montreal, QC, Canada, since 1993, and Chair of the department since 2006. He is the Director and Principal Investigator of the Centre for Advanced Systems and Technologies Communications at McGill University. During the 2000 to 2001 academic years, he took a leave of absence from McGill University to become the Director of Optical Integration at Accelight Networks, Pittsburgh, PA. His research interests include optoelectronic-VLSI, analog circuits for communications, electro-optic switching devices, and optical network design including OCDMA, radio-over-fiber, and agile packet switched networks. Dr. Plant has received five teaching awards from McGill University, including most recently the Principal's Prize for Teaching Excellence in 2006. He is a James McGill Professor and an IEEE LEOS Distinguished Lecturer. He was the recipient of the R.A. Fessenden Medal and the Outstanding Educator Award, both from IEEE Canada, and received a NSERC Synergy Award for Innovation. He is a member of Sigma Xi, a Fellow of the Optical Society of America, and a Fellow of the IEEE.