

Experimental Demonstration of a SAC-OCDMA PON With Burst-Mode Reception: Local Versus Centralized Sources

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Abstract—In this paper, we demonstrate experimentally the uplink of a 7×622 Mb/s incoherent spectral amplitude coded optical code-division multiple access (SAC-OCDMA) passive optical network (PON) with burst-mode reception. We consider two network architectures: local sources (LS) at each optical network unit (ONU) versus a single source located at the central office. We examine both architectures over a 20-km optical link, as well as a reference back-to-back configuration. Our architectures can adopt two-feeder and single-feeder topologies; however, we only test the two-feeder topology and therefore the effect of Rayleigh backscattering is neglected. We also study the relative merits (cost and performance) of local sources versus centralized architectures. A penalty of less than 2 dB between the LS and the centralized light sources (CLS) architectures was measured at a bit error rate (BER) of 10^{-9} under certain assumptions on the relative power of the sources. The power budget in the CLS architectures is more critical than in the LS architectures; extra splitting and propagation losses exist as the uplink travels through the network back and forth. Doubling the number of users while maintaining the same distance and source power in LS architectures imposes 3-dB additional losses, whereas for CLS architectures, there are 6-dB extra losses. CLS architectures can overcome these penalties using amplification at the central office. Alternately, central office amplification can be used to more than double the number of users in LS SAC-OCDMA PONs. A standalone (no global clock) burst-mode receiver with clock and data recovery (CDR), clock and phase alignment (CPA), and Reed–Solomon RS(255,239) forward-error correction (FEC) decoder is demonstrated. A penalty of less than 0.25 dB due to the nonideal sampling of the CDR is reported. The receiver also provides an instantaneous phase acquisition time for any phase step between consecutive packets, and a good immunity to silence periods. A coding gain of more than 2.5 dB was reported for a single-user system, and BER floors were completely eliminated. Error-free transmission ($\text{BER} < 10^{-9}$) for a fully loaded PON was achieved for the LS architecture as well as the CLS architecture. Continuous and bursty upstream traffic were tested. Due to the CPA algorithm, even with zero preamble bits we report a zero packet loss ratio

(PLR) for up to four simultaneous users in case of bursty traffic, and more than two orders of magnitude improvement in the PLR for fully loaded PON systems.

Index Terms—Burst-mode receiver, clock-and-data recovery (CDR), clock-and-phase alignment (CPA), forward-error correction (FEC), frequency encoding, intensity noise, passive optical network (PON), spectral amplitude coded optical code-division multiple access (SAC-OCDMA).

I. INTRODUCTION

PASSIVE optical networks (PONs) are recognized as an economic and future solution to alleviate the bandwidth bottleneck in the access network [1]–[4]. A PON typically has a physical tree topology with an optical line terminal (OLT) located at the root and optical network units (ONUs) connected to the branches. Existing PON standards are based on time division multiplexing (TDM) and can serve up to 32 or 64 users at an aggregate bit rate of 1.25 Gb/s [1]. In order to handle future bandwidth demands, many researchers considered wavelength division multiplexing (WDM) to increase the capacity of these existing PONs [5]–[8]. However, some limitations to WDM PONs market penetration exist. Adoption of WDM PONs requires upgrading the infrastructure from passive splitters to passive wavelength routers. The use of coherent laser sources in such PONs adds to the cost and complexity of the system, requiring external circuits for laser stabilization. Other solutions that combine subcarrier multiplexing (SCM) to WDM were proposed to make use of the same wavelength for both uplink and downlink [9], [10]. In this case, more electrical circuits containing with local oscillators and mixers are required. Using TDM over WDM PONs helps increase the capacity further, but requires synchronization [11].

Optical code-division multiple access (OCDMA) combines the large bandwidth of the fiber medium with the flexibility of the CDMA technique to achieve high-speed connectivity [12]. A promising approach for upgrading existing PONs, or for next generation PONs, is the use of OCDMA with its simple ONU and OLT configurations requiring no synchronization [13]–[15]. PON infrastructures (i.e., passive splitters) need not to be upgraded to adopt OCDMA. Other attractive features of OCDMA include all-optical processing, truly asynchronous transmission, bandwidth efficiency, soft capacity on demand, protocol transparency, simplified network control, and flexibility on controlling the quality of service (QoS) [12], [13].

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In this paper, we focus on incoherent spectral amplitude-coded optical code-division multiple access (SAC-OCDMA) as a solution for PONs, because of its ability to cancel multiple access interference (MAI), and to permit the use of low-speed electronics operating at the bit rate [15], [16]. Furthermore, advances in writing fiber Bragg gratings (FBGs) make possible the design of low-cost and compact passive encoders/decoders well adapted to PONs [15], [17]. In our work, we examine several PON physical architectures, namely, the use of local sources at each ONU versus the use of a single light source housed at the central office. An inexpensive incoherent light source is placed either at each ONU or at the OLT, for the local source (LS) architecture or the centralized light source (CLS) architecture, respectively. In order to manage uplink (from users to OLT) and downlink (from OLT to users) traffic, we consider both two-feeder and single-feeder approaches [11].

Much research into OCDMA focuses on optical design, while assuming the availability of high-speed electronics [12]–[15]. Emerging research is concerned with the electronic design of receivers for optical multiaccess networks, featuring postprocessing functionalities [18], [19]. Previous electronic receivers were reported in the literature for fast-frequency hop (FFH) OCDMA and PON systems [20], [21]. FFH-OCDA (or λ -t OCDMA) requires electronics that operate at the chip rate rather than the data rate. SAC-OCDA has the advantage of operating at the data rate, and enjoys excellent MAI rejection with balanced detection. In this paper, we demonstrate experimentally burst-mode reception of an incoherent SAC-OCDA PON uplink supporting seven asynchronous users at 622 Mb/s (FFH results were at 155-Mb/s data rate). Our receiver has no global clock (i.e., synchronization), instead exploiting a commercial SONET clock-and-data recovery (CDR). Reed–Solomon RS(255,239) forward-error correction (FEC) is also implemented on a field-programmable gate array (FPGA). The receiver features clock-and-phase alignment (CPA) and includes a custom bit error rate tester (BERT) implemented on the FPGA.

Different PON architectures are tested experimentally, and bit error rate (BER) and packet loss ratio (PLR) are measured. The immunity of the CDR in terms of consecutive identical digits (CID) is also measured. We simulate the BER with FEC in order to validate our measurements. We quantify the increase in soft capacity via FEC, while working with a nonideal recovered clock that provides realistic, achievable sampling. We also present and analyze the cost and power budget (uplink direction) of both LS and CLS SAC-OCDA PON architectures.

The rest of this paper is organized as follows. Section II is concerned with the SAC-OCDA PON physical topologies. We present and compare different OCDMA PON architectures including LS versus CLS architectures, and two-feeder versus single-feeder architectures. Section III is devoted to the description of the burst-mode receiver functionalities. The operation of the CDR, CPA, FEC, and the FPGA-based BERT are outlined there. Our experimental setup, as well as the results, are presented and discussed in Section IV. In Section V, we consider the performance and cost tradeoffs of the LS versus the CLS

solution for SAC-OCDA PONs. Finally, this paper is summarized and concluded in Section VI.

II. SAC-OCDA PON ARCHITECTURES

Tree architectures are widely used for fiber-to-the-home (FTTH), or the so called “last mile” market. Such networks referred to as PONs employ only passive components (couplers, circulators, etc.) in the optical distribution network (ODN) and at the remote node (RN), and they have low installation and management costs. Different PON architectures have been proposed by different research groups [5]–[11], including both two-feeder and single-feeder architectures to multiplex uplink and downlink traffic. In two-feeder architectures, uplink and downlink traffic is sent independently on separate feeders; a single-feeder architecture carries both uplink and downlink on one fiber. Although single-feeder topologies reduce infrastructure and maintenance costs, they suffer from Rayleigh backscattering if the same wavelength is used for upstream and downstream. Two-feeder architectures give the flexibility to use the same wavelength band for upstream and downstream, making the design easier. Although our OCDMA PON architectures offer the flexibility of adopting both two-feeder and single-feeder architectures, we test only the two-feeder architecture for experimental convenience. The effects of Rayleigh backscattering, which are reduced in such architectures, are then not addressed.

In this paper, we propose four different architectures for SAC-OCDA PONs as illustrated in Fig. 1; both LS architectures [Fig. 1(a)] and CLS architectures [Fig. 1(b)] can exist with two-feeder and single-feeder topologies (shown within the ODN). We analyze both architectures with each feeder topology in terms of power budget, but we experimentally test only the two-feeder topology. Although our architectures provide full-duplex communications, we focus on the design of the ONU side, as it is one of the most challenging factors in PON design [1]–[4], [21]. More specifically, we focus on the design of the ONU transmitter (uplink transmitter). The optimum receiver for a SAC-OCDA PON at both the OLT and ONU is the conventional balanced receiver because of its ability to suppress first-order MAI. The structure of such a receiver for the ONU is given in Fig. 1, including a 1×2 coupler, a decoder (DEC), a complementary decoder ($\overline{\text{DEC}}$), and a balanced photodiode (PD). Fiber Bragg gratings working in transmission are used as the encoders/decoders because of their good group delay performance, which is vital in SAC-based OCDMA systems [15]. Fig. 1(a) shows the proposed LS SAC-OCDA PON; in that case, an inexpensive directly modulated light emitting diode (LED) or a broadband erbium-based source is externally modulated and located at each ONU. On the other hand, the proposed CLS SAC-OCDA PON, shown in Fig. 1(b), places a single powerful source at the OLT with remote external modulation of that source at each ONU. In CLS architecture, coarse WDM filters are needed at the OLT and ONU, as shown in Fig. 1(b), to separate the continuous wave light for the uplink from the modulated downlink. Such filters can be replaced by passive couplers if the same wavelength band is used for both downlink and uplink. The RN, the ODN, and the OLT multiuser transmitter/receiver are similar for the two architectures. The

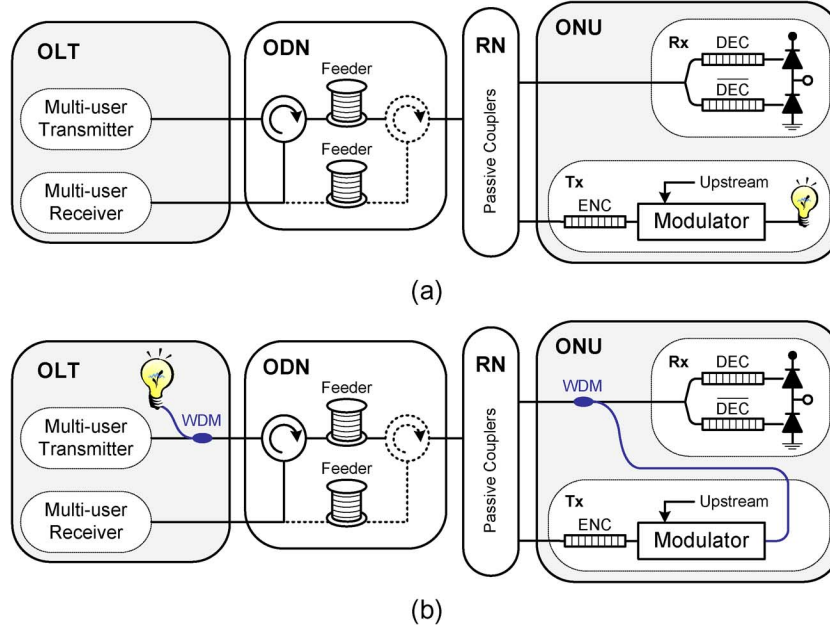


Fig. 1. SAC-OCDMA PON physical architecture: (a) LS architecture; (b) CLS architecture.

RN consists of passive combiners and splitters, as in existing TDM PONs, so there is no need to upgrade the PON infrastructure; for WDM PONs, the couplers must be replaced by arrayed waveguide gratings (AWGs). The RN serves as a connection between the ONUs and the ODN. Users are connected to the RN through short length fibers (~ 1 km) called distribution drop fibers. The ODN, composed of feeder fibers (~ 20 km) and passive optical circulators, can adopt a two-feeder (the second feeder with its corresponding circulator shown in dotted in Fig. 1) or a single-feeder architecture. At the OLT, a multiuser transceiver is used to communicate with all the users in both directions. The OLT should contain optical amplifiers to compensate for the losses through the network and also for the combining and splitting losses of the multiuser transmitter and receiver when implemented all optically (the same design as ONUs in Fig. 1). Note that electronic implementation of OLT transceivers could help reduce the loss budget significantly by eliminating the optical couplers. Furthermore, all preprocessing and postprocessing functionalities could be easily handled in electronics.

The uplink power budget of the proposed PON architectures in Fig. 1 is mainly affected by the RN and the ODN adopted. In LS architectures [see Fig. 1(a)], the uplink signal travels only in one direction, from the ONU to the OLT. For N ONUs (corresponding to a $1 : N$ splitting ratio), we have $10 \log(N)$ dB splitting losses, in addition to the propagation losses through one feeder and the insertion losses of a three-port circulator. These observations are valid for both the two-feeder or the single-feeder topology. In the CLS architecture, shown in Fig. 1(b), for uplink, the unmodulated source travels from the OLT to the ONU and after modulation returns to the OLT. Therefore, a CLS PON experiences twice the ODN and RN losses (splitting losses + propagation losses + insertion losses) as a similar LS PON, again whether the two-feeder or the single-feeder topology is

used. We will discuss in Section V the performance and cost tradeoffs of the LS versus the CLS solution.

III. SAC-OCDMA BURST-MODE RECEIVER

According to the PON standards, a continuous downlink in the wavelength band of 1480–1500 nm carries TDM data, or OCDMA encoded data in our case, from the OLT towards multiple ONUs. A burst-mode link in the 1310-nm window collects all ONUs upstream traffic toward the OLT as variable-length packets at the same rate. Because of the bursty nature of the upstream, the OLT receives packets from active ONUs with different amplitude levels and phases. In class B PONs, the average signal level may vary 21 dB in the worst case from packet to packet [21]. These packets are of variable length and are interleaved with a guard time of only four bytes as specified by the physical medium-dependent (PMD) layer [21], [22].

A typical burst-mode uplink signal that complies with PON standards is used as a test signal in our experiments and is shown in Fig. 2(a). Packet 1 serves as a dummy packet to force the burst-mode CDR to lock to a certain phase (ϕ_1) before the arrival of packet 2. A silence period including m CIDs and a phase step $\Delta\phi$ is inserted between the two packets. This idle period also represents the asynchronous nature of OCDMA due to the random phase step $-2\pi \leq \Delta\phi \leq +2\pi$ between the two packets. The PLR measurements and their corresponding BER measurements are performed only on packet 2, which consists of n preamble bits, 20 delimiter bits, $2^{15} - 1$ payload bits, and 48 comma bits. The preamble and the delimiter bits correspond to the physical layer upstream burst-mode overhead at 622 Mb/s, as specified by the ITU-T G.984.2 standard [22]. The preamble bits are used to perform phase recovery. The delimiter is a unique pattern indicating the start of the packet to perform byte synchronization. Similarly, the comma is a unique

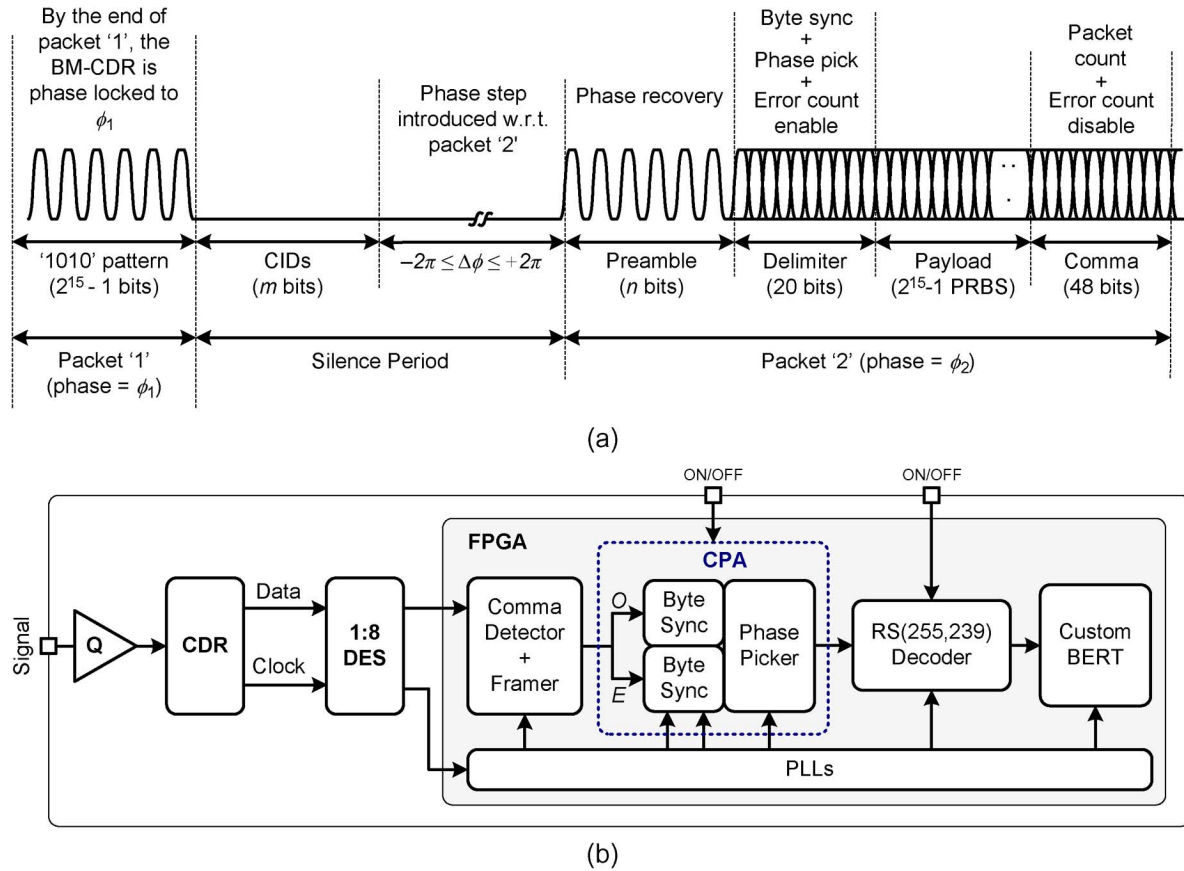


Fig. 2. (a) Typical burst-mode uplink test signal used to test the phase acquisition time of the clock phase aligner. (b) Block diagram of the OLT burst-mode receiver for SAC-OC DMA PONs (DES: deserializer; Sync: synchronizer).

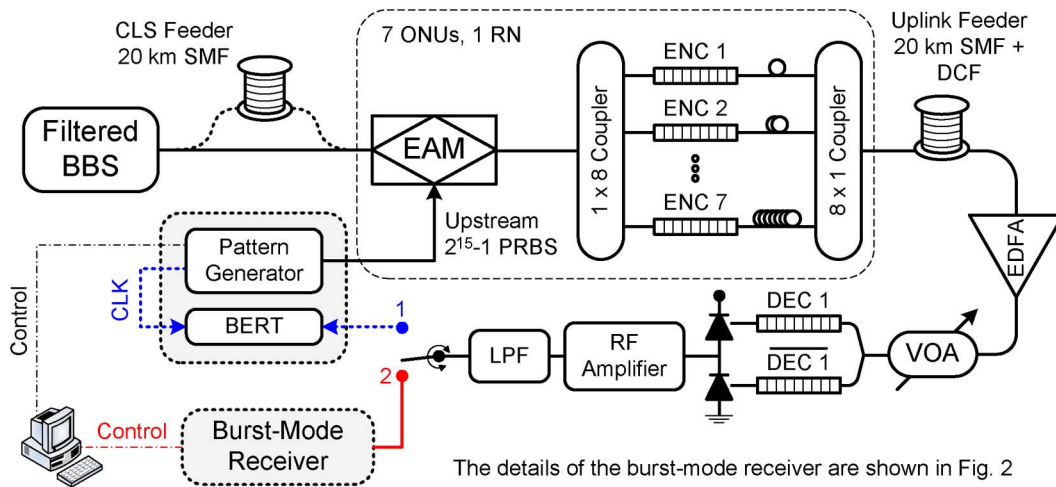


Fig. 3. Experimental setup for a 7 x 622 Mb/s SAC-OC DMA PON uplink (BERT: BER tester; CLK: clock; DEC: decoder; and ENC: encoder).

pattern to indicate the end of the payload. The payload is simply a $2^{15} - 1$ pseudorandom binary sequence (PRBS). The BER and PLR are measured for the payload bits only. The lock acquisition time corresponds to the number of bits (n) in front of the delimiter in order to get a zero PLR for over 3 min at 622 Mb/s ($> 10^6$ packets received, i.e., $PLR < 10^{-6}$), a $BER < 10^{-10}$, and for any phase step ($-2\pi \leq \Delta\phi \leq +2\pi$) between consecutive packets [19]. We will demonstrate that even

at $n = 0$, i.e., no preamble bits, our phase picker gives excellent results. To generate alternating packets with adjustable phase, as in Fig. 2(a), we combined two programmable ports from the HP80000 pattern generator shown in Fig. 3 using a radio frequency (RF) power combiner. The phase steps between the consecutive packets can be set anywhere between ± 2 ns on a 2-ps resolution, corresponding to a ± 1.25 unit interval (UI) at 622 Mb/s. Note that 1 UI corresponds to 1-bit period.

A. Building Block Diagrams

The main building blocks of the SAC-OCDDMA burst-mode receiver we designed are illustrated in Fig. 2(b). The receiver includes a multirate SONET CDR from Analog Devices (Part #ADN2819), a 1:8 deserializer from Maxim-IC (Part #MAX3885), and a CPA module and a FEC RS(255,239) decoder implemented on a Virtex II Pro FPGA from Xilinx. Our receiver without the CPA is therefore similar to that in [20], but without the return-to-zero (RZ) to nonreturn-to-zero (NRZ) converter needed for FFH-OCDDMA. The receiver also avoids the use of an 8:1 serializer (used with FFH-OCDDMA) to up convert the frequency. The quantizer (Q) is used before the CDR to threshold the incoming signal to filter out intensity noise and other channel impairments. The threshold is manually adjusted to sample in the middle of the eye opening to obtain the optimum BER. The multirate CDR then recovers the clock and data from the incoming signal. The receiver is operated at either 622 or 666.43 Mb/s depending on whether the FEC module is OFF or ON, respectively. The CDR is followed by a 1:8 deserializer (DES) that reduces the frequency of the recovered clock and data to a frequency that can be processed by the digital logic. Afterwards, a framer, a comma detector, a CPA (including a phase picker and byte synchronizers), phase locked loops (PLLs), an RS(255,239) decoder, and a custom BERT are implemented on an FPGA. Note that a computer is used to control the output of the pattern generator and to communicate with the FPGA on the receiver (Fig. 3). Automatic detection of the payload is implemented on the FPGA through a comma detector and a framer, which are responsible for detecting the beginning (delimiter bits) and the end (comma bits) of the packets, respectively, as in [20]. The CPA module makes use of the phase picking algorithm in [19] and the CDR operating at $2\times$ oversampling. The CPA is turned ON for the PLR measurements with phase acquisition; otherwise, it is bypassed. The CPA is then followed by the RS decoder and the FPGA-based BERT.

B. Burst-Mode Receiver Functionalities

The idea behind the CPA is based on the simple, fast, and effective algorithm in [19]. Since the CDR samples the data twice per bit, the odd samples and even samples [O and E , respectively, in Fig. 2(b)], sampled on the alternate (odd and even) clock rising edges (t_{odd} and t_{even} in Fig. 12) are identical. The odd samples are forwarded to path O and the even samples to path E . The byte synchronizer is responsible for detecting the delimiter. It makes use of a payload detection algorithm to look for a preprogrammed delimiter. The idea behind the phase picking algorithm is to replicate the byte synchronizer twice in an attempt to detect the delimiter on either the odd and/or even samples of the data, respectively. That is, regardless of any phase step, i.e., $-2\pi \leq \Delta\varphi \leq +2\pi$, between consecutive packets, there will be at least one clock edge (either t_{odd} or t_{even}) that will yield an accurate sample. The phase picker then uses feedback from the byte synchronizers to select the correct path from the two possibilities. For further illustration, we refer the reader to Fig. 12, where the CDR output for the $2\times$ over sampling mode at specific three possible phase differences between consecutive packets is shown.

The realigned data is sent to the RS(255,239) decoder which is turned on for BER measurements with FEC; otherwise, it is bypassed [Fig. 2(b)]. The RS decoder is an IP core from the Xilinx LogiCORE portfolio. The FPGA-based BERT designed in [19] is implemented to selectively perform BER and PLR measurements on only the payload of the packets. The BERT compares the incoming data with an internally generated $2^{15} - 1$ PRBS. This eliminates the need to up convert the frequency back to 622 or 666.43 Mb/s using an 8:1 serializer after the FPGA, and avoids the use of a commercial BERT. Note that conventional BERTs require a continuous alignment between the incoming pattern and the reference pattern, and milliseconds to acquire synchronization. The phase step response of the burst-mode CDR can make conventional BERTs lose pattern synchronization at the beginning of every packet while the sampling clock is being recovered by the CDR. The custom BERT does not require fixed synchronization between the incoming pattern and the reference pattern of the error detector. Synchronization happens instantaneously at the beginning of every packet, therefore enabling PLR measurements on discontinuous, bursty data.

IV. EXPERIMENTAL SETUP, RESULTS, AND DISCUSSIONS

A. Experimental Setup

The experimental setup illustrated in Fig. 3 is used to test the uplink of the LS and CLS SAC-OCDDMA PON architectures shown in Fig. 1, using only the two-feeder topology. A single incoherent broadband source (BBS) is filtered around 1542.5 nm using two cascaded FBG bandpass filters providing a 9.6-nm band, and serves to test both the CLS and LS architectures. An NRZ $2^{15} - 1$ PRBS is input to a single polarization independent electroabsorption modulator (EAM) that, in conjunction with appropriate decorrelating delay lines, represents independent data streams each modulated externally at a distinct ONU. For the CLS architecture, the single powerful BBS is sent over the 20-km CLS/downlink feeder and is then split by the first 1×8 coupler representing the RN. For the LS architecture, the 20-km single-mode fiber (SMF-28) is not present and the first 1×8 coupler is not part of the network, but rather an experimental trick to emulate eight separate, low power incoherent sources. The balance of the setup is interpreted as seven ONUs each with a distinct CDMA encoder, followed by the second 1×8 coupler representing the RN and a 20-km SMF for the uplink in the two-feeder architecture. We did not use the circulators and the WDM filter in Fig. 1, as we were only testing the uplink; these components would only contribute to insertion losses.

At the OLT, an appropriate dispersion compensation fiber (DCF) is used, and the signal is amplified by an erbium-doped fiber amplifier (EDFA) and detected in a balanced receiver. A variable optical attenuator (VOA) serves to control the received power level. A balanced detection scheme similar to that in Fig. 1 is then used to decode user 1. To ensure good detection and MAI cancellation, the optical lengths of the two branches of the receiver are perfectly adjusted; furthermore, the power at both arms due to MAI is controlled using another VOA (not shown in Fig. 3) that accounts also for the splitting ratio of the 1×2 coupler as in [15]. After decoding, each arm goes

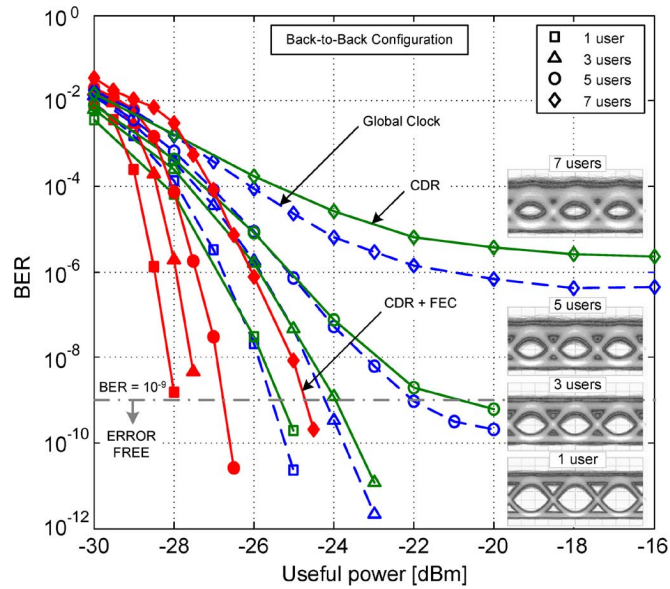


Fig. 4. BER versus useful power for back-to-back configuration (dashed lines for global clock; solid lines and unfilled markers for CDR; solid lines and filled markers for CDR with FEC).

into one of the two separate inputs of an 800-MHz balanced photodiode from New Focus (model 1617). The electrical signal is then amplified (MITEQ, 0.01–500 MHz) and low-pass filtered by a fourth-order Bessel-Thomson filter (Picosecond, 467 MHz) to remove the out-of-band high-frequency electrical noise. Such a filter reduces intensity noise from the incoherent broadband source [15], while keeping intersymbol interference to a minimum. Measurements are then performed with either a global clock, or through our OCDMA burst-mode receiver, corresponding to switch position 1 or 2, respectively. The desired information rate per user is 622 Mb/s; an RS(255,239) code introducing 15/14 overhead leads to an aggregate bit rate of 666.43 Mb/s. The spectral coding is achieved by FBGs working in transmission; balanced incomplete block design (BIBD) codes with length 7 and weight 3 are used as in [15].

B. Experimental Results

In this section, we present the system performance in terms of BER, PLR, and the CID immunity for the back-to-back configuration (without fiber link), and the LS and the CLS SAC-OCDMA PON architectures. The experimental results are presented in Figs. 4–11, except for Fig. 8, which shows simulation versus measurement results. We present also the power and link budget for the different architectures that were tested. BER measurements are reported for continuous upstream traffic, while PLR is reported for packet data, based on the burst-mode BERT results. PLR measurements use bursty traffic [similar to that in Fig. 2(a)] with packets of $2^{15} - 1$ bits length and zero preamble length; use of a preamble would improve PLR, but at the cost of reduced throughput. Today's PON standards provide for a maximum preamble length of 28 bits [22], to allow the receiver enough time to recover the clock, adjust the phase, and control the gain. The operation of the CDR and its ability to provide a clock signal with a $2\times$ oversampling, which is used by the phase

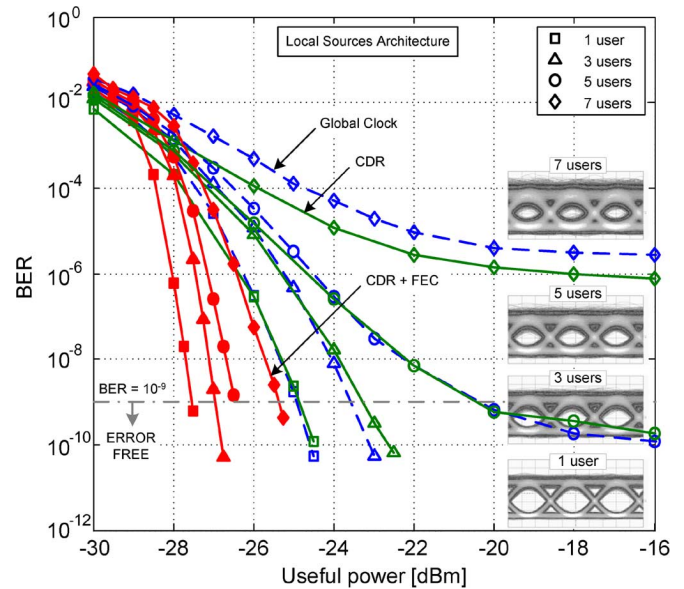


Fig. 5. BER versus useful power for LS architecture (dashed lines for global clock; solid lines and unfilled markers for CDR; solid lines and filled markers for CDR with FEC).

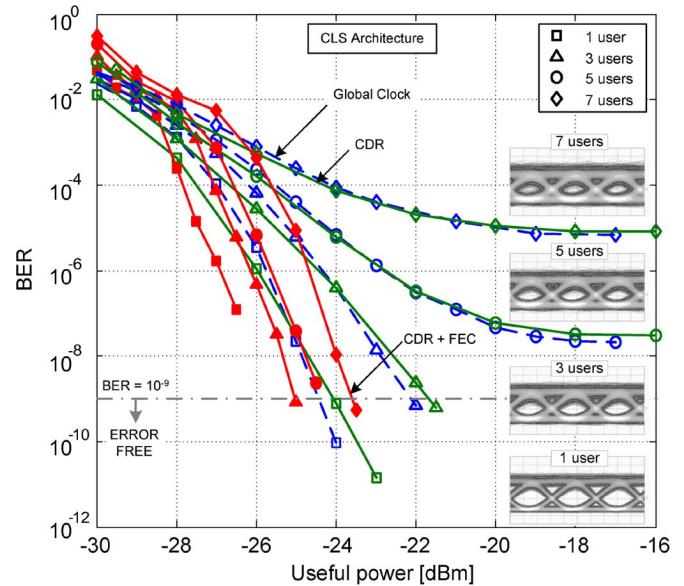


Fig. 6. BER versus useful power for CLS architecture (dashed lines for global clock; solid lines and unfilled markers for CDR; solid lines and filled markers for CDR with FEC).

picking algorithm, is explained in Fig. 12 through a set of measured eye diagrams.

In Fig. 4, we present the BER versus power for the back-to-back configuration. The horizontal axis represents the useful power, i.e., the received power from the desired user. Curves are presented for a single-user system up to a fully loaded system of seven users. Ignoring for a moment the solid curves with filled markers (FEC results), we focus our attention on the set of curves for the global clock (dashed) and for the CDR module (solid + unfilled markers). Starting from a single user, we see a classic waterfall curve; as we go to a fully charged system of seven users, BER floors begin to appear, starting from five

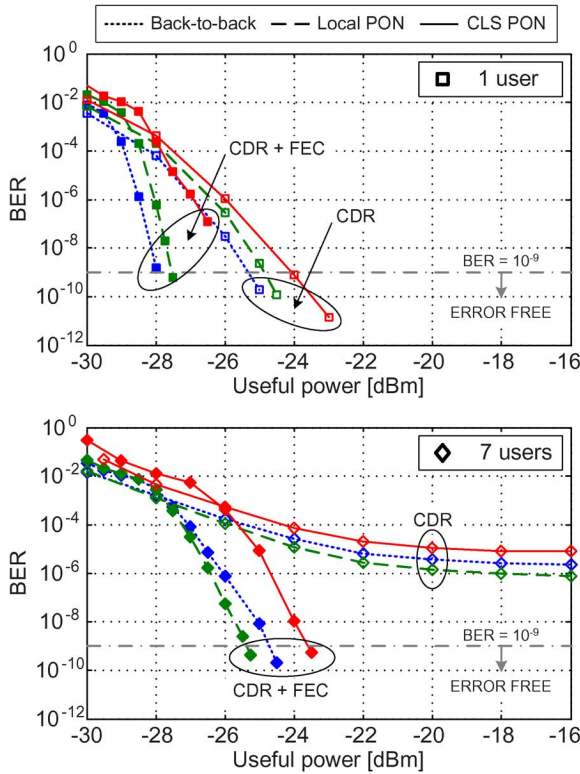


Fig. 7. BER versus useful power for a single-user and fully loaded systems (dotted lines for back-to-back; dashed lines for LS architecture; solid lines for CLS architecture).

users. The penalty when using the CDR unit is not significant (less than 0.25 dB), as we can see by the proximity of the CDR and global clock curves. When adding the FEC to the CDR operation, we see that all BER floors disappear and we return to the classic waterfall close to the single-user performance. Eye diagrams measured at -18 dBm are included as insets in Fig. 4. The single-user eye diagram is very open, while the fully loaded system with seven users has a severely closed eye. Despite the eye closure, the FEC allows us to return to error free performance.

Similar curves for the LS and CLS PON architectures are presented in Figs. 5 and 6, respectively. The same trends are observed, except for the case of seven users for the LS PON architecture. In that case, we note a slight improvement in the performance with the CDR compared to the global clock measurement, despite the nonideal sampling of the CDR. This improvement is related to the threshold adjustment, as in [20]. At small power levels, we were able to manually control the decision threshold [using a direct current (dc) power supply] to great accuracy for the CDR measurements, while we were limited by the automated decision threshold in the commercial BERT for global clock measurements. The manual optimization explains the slight improvement in the performance when using the recovered clock especially at lower power levels; this explains the crossings of the global clock curves with the CDR curves at around -26 dBm for the three measurement configurations in Figs. 4–6.

For easier comparison of the back-to-back configuration and the two PON architectures, we plot in Fig. 7 the single-user and

fully loaded (seven users) systems BER curves. We consider the performance using our burst-mode receiver when the FEC module is OFF (curves with unfilled markers), and when it is ON (curves with filled markers). A coding gain of more than 2.5 dB (measured at $\text{BER} = 10^{-9}$) is observed for a single user for the three architectures. Furthermore, the penalty from a back-to-back configuration to the LS PON is negligible (less than 0.25 dB), as well as the one from a LS PON to the CLS PON architecture. Results are consistent with that in [15] for a back-to-back configuration and a 20-km communication link. For the seven-users case, we see clearly all BER floors are eliminated by the FEC. Operating at a relatively low power (-23 dBm received power) we obtain error free transmission ($\text{BER} \ll 10^{-9}$) for the three architectures. Therefore, we were able to demonstrate for the first time to our knowledge an error-free 7×622 Mb/s uplink of an incoherent SAC-OCDMA PON (LS and CLS architectures were tested) using a standalone burst-mode receiver with CDR and FEC.

Finally, in Fig. 7, we can compare the performance of LS and CLS architectures under our assumption of an 8 : 1 ratio of the relative power of the centralized to the local sources. A penalty of less than 2 dB was measured for LS at a BER of 10^{-9} when FEC and CDR were in use. Recall that this penalty is for the particular instance of a network of eight users, and an 8 : 1 ratio of relative power. We will discuss later how to generalize these results.

Simulation versus measurement of the BER using FEC for the three different configurations is shown in Fig. 8. Let P_B be the measured BER without FEC in Fig. 4, Fig. 5, and Fig. 6 for the various scenarios. Organizing the bits in symbols of m bits yields an equivalent symbol error rate of

$$P_S = 1 - (1 - P_B)^m. \quad (1)$$

The RS(255,239) FEC uses 8-bit symbols and, in a memoryless channel, can correct up to $t = 8$ symbol errors per frame (239 uncoded symbols), yielding a symbol error rate after FEC of [23]

$$P_{S_FEC} \approx \frac{1}{2^m - 1} \sum_{j=t+1}^{2^m-1} j \binom{2^m-1}{j} P_S^j (1 - P_S)^{2^m-1-j}. \quad (2)$$

Again assuming a memoryless channel, the BER P_{B_FEC} is about one half this symbol error rate, as we are using orthogonal signaling (ON–OFF keying) [23]. We plot the memoryless channel prediction for P_{B_FEC} and our measurement in Fig. 8. There is one order of magnitude mismatch between simulation and measurements; our predictions are too optimistic. This is more likely due to the memory added to the channel through the BBS (intensity noise), the CDR, and other components.

In Fig. 9, we plot the PLR versus the phase difference between packets for the three configurations under test when using the SONET CDR without the phase picking algorithm. The power level was kept at -18 dBm for these and all subsequent measurements. Bursty traffic identical to that in Fig. 2 with zero preamble bits is generated for all users. We will demonstrate that our phase picker does not require any preamble bits for phase acquisition. We consider that all packets are correctly received

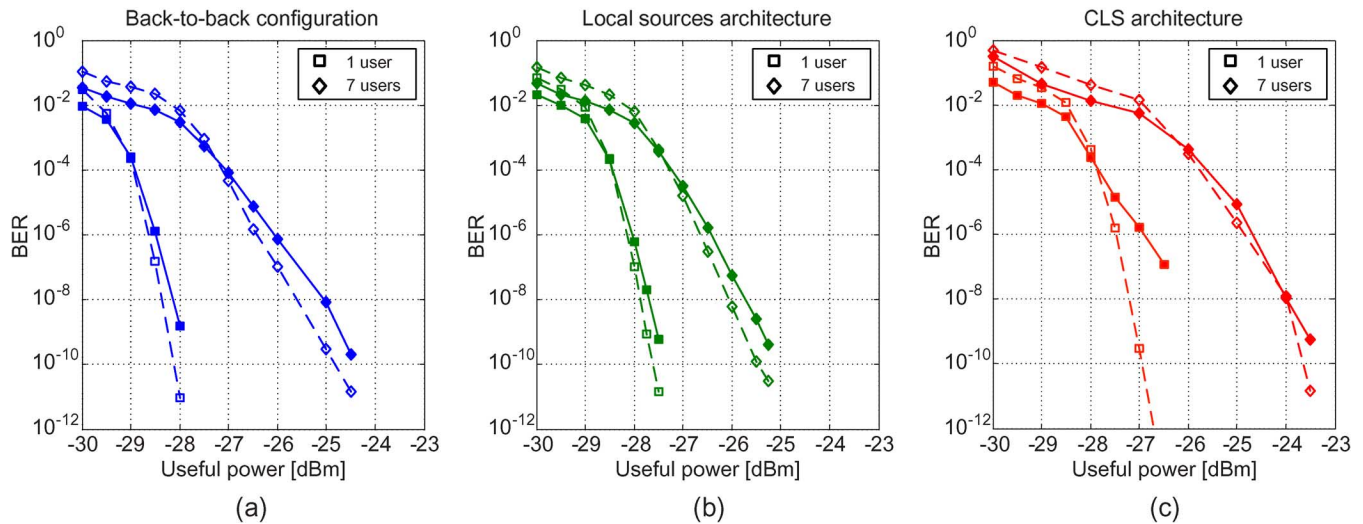


Fig. 8. Simulated and measured BER versus useful power for different configurations (dashed lines for simulated BER; solid lines for measurements): (a) back-to-back configuration; (b) LS architecture; (c) CLS architecture.

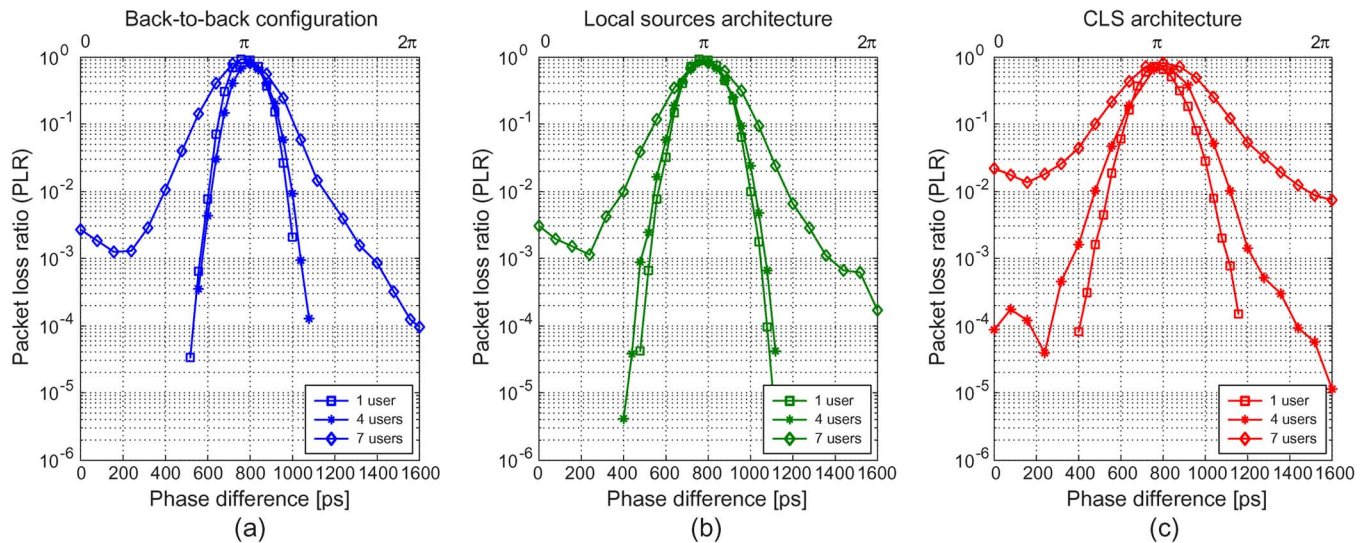


Fig. 9. PLR versus phase difference without CPA for different number of users: (a) back-to-back configuration; (b) LS architecture; (c) CLS architecture.

when $PLR < 10^{-6}$, corresponding to a $BER < 10^{-10}$. We have restricted the horizontal axis to values from 0 to 1600 ps, corresponding to 0 to 2π phase difference at the desired bit rate (~ 622 Mb/s). We did not consider the interval from -2π to 0, because it gives theoretically the same performance as the positive interval [19]. We observe bell-shape curves for PLR centered around 800 ps; 800 ps corresponds to a phase shift of π radians, i.e., the worst case. Jitter would have led to the worst case phase (π rad) being displaced from 800 ps, hence we conclude that jitter is not significant in our measurements. At relatively small phase shifts (near 0 or 2π rad), we note that for a single-user system we can easily achieve zero PLR with the CPA module disabled, because the CDR is almost sampling at the middle of each bit (refer to Fig. 12 for the conventional CDR output when the phase shift is 0 rad). By comparing the curves on the same subplot, i.e., for each configuration, we note the degradation in performance passing from a single-user system to a fully loaded network of seven users. There is also a penalty

when passing from the back-to-back configuration to the LS PON and then to the CLS PON, when comparing curves on different subplots. The degradation in the PLR can be explained by the corresponding degradation in the BER. As the BER performance degrades, there is a higher chance of having erroneous bits in the packet delimiter. With the delimiter not being correctly detected, a packet is declared lost, hence contributing to the packet loss count.

In order to show the improvement that can be achieved using the CPA functionality of our SAC-OCDMA burst-mode receiver, we have plotted in Fig. 10 the worst case PLR, i.e., the maximum PLR value that occurs at π phase shift, against the number of users for the three configurations, with and without CPA. In the case of CDR without CPA, the worst case PLR is near 1 (see Fig. 9), as it corresponds to the receiver sampling at the edge of the eye diagram. In contrast, the phase picking algorithm samples each bit twice, within the eye, and significantly enhances the performance. With the CPA, no packets

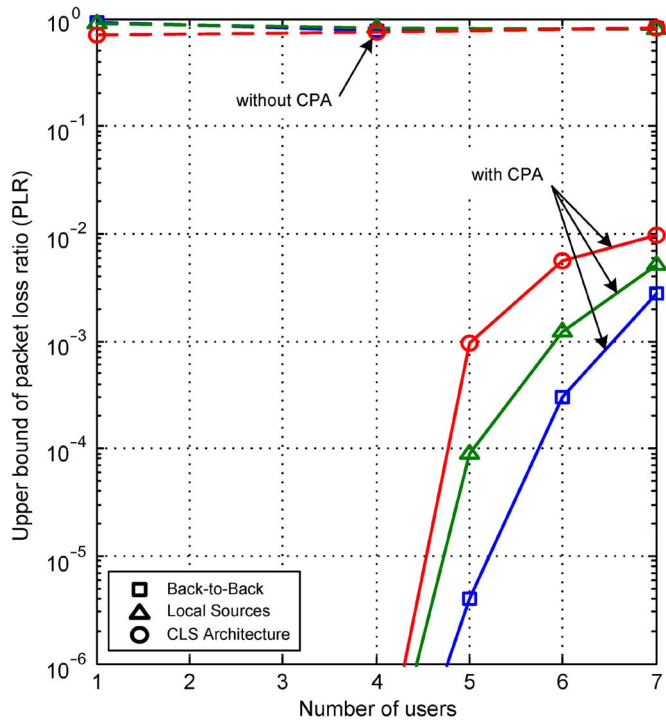


Fig. 10. PLR versus number of users for different PON architectures (dashed lines for the system without CPA; solid lines for the system with CPA).

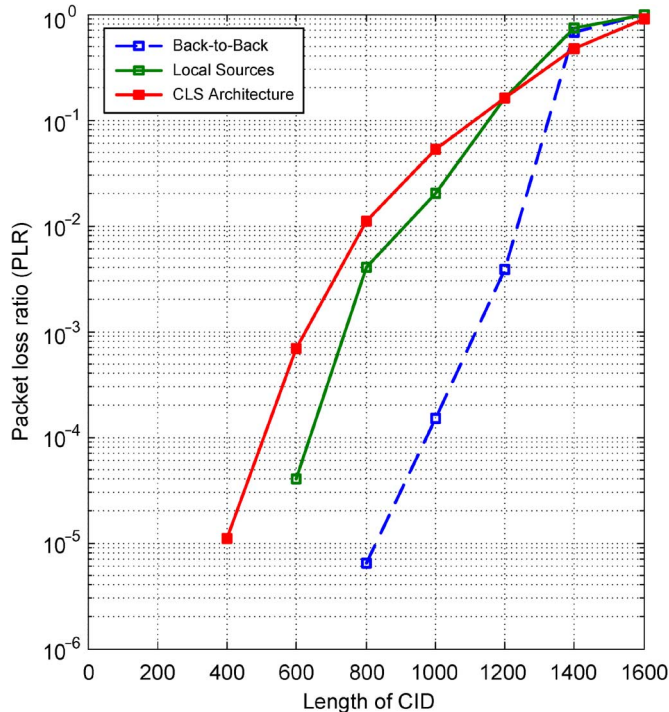


Fig. 11. PLR versus length of CID for different PON architectures.

are for lost up to four users for the three different architectures ($PLR < 10^{-6}$). Increasing the number of users beyond four deteriorates the BER and thus the PLR. For a fully loaded PON of seven users, the CPA algorithm can improve the performance by more than two orders of magnitudes.

The immunity of the CDR to silence periods is examined in terms of the CID length in Fig. 11, showing the PLR for the

single-user case for the back-to-back configuration, and the LS and CLS architectures. Recall that the useful power is still kept at -18 dBm and that the packets do not contain any preamble bits. The maximum length of CIDs can reach roughly 400, 600, and 800 bits for the CLS, LS, and the back-to-back configurations, respectively. A maximum of 200 bits of CIDs would guarantee zero packet loss for the three configurations; therefore, our SAC-OCDMA burst-mode receiver meets all existing PON standards.

Fig. 12 shows the response of the CDR to bursty traffic, as well as the $2\times$ oversampling mode of the CDR and the CPA operation. Three specific phase differences between packets are considered: (a) no phase difference $\Delta\varphi = 0$ rad (0 ps); (b) $\Delta\varphi = \pi/2$ rad (400 ps); and (c) $\Delta\varphi = \pi$ rad (800 ps). Whereas $\Delta\varphi = \pi$ rad (800 ps) represents a worst case phase step for the CDR operated at the bit rate, $\Delta\varphi = \pi/2$ rad (400 ps) phase step is the worst case scenario for the over sampling CDR at $2\times$ the bit rate. The $2\times$ oversampling mode produces two samples per bit, which helps the CPA algorithm locking to the correct phase of the incoming packet. To understand how the CPA works, consider the case when there is no phase step ($\Delta\varphi = 0$ rad); path O correctly samples the incoming pattern [see t_{odd} in Fig. 12(a)]. For phase step $\Delta\varphi = \pi/2$ rad (400 ps), path E will sample the bits on or close to the transitions after the phase step. In this situation, the byte synchronizer of path E will likely not detect the delimiter at the beginning of the packet. On the other hand, the byte synchronizer of path O will have no problems detecting the delimiter [see t_{odd} in Fig. 12(b)]. The phase picker controller monitors the state of the two byte synchronizers and selects the correct path accordingly (path O in this particular case). Once the selection is made, it cannot be overwritten until the comma is detected, indicating the end of the packet. This process repeats itself at the beginning of every packet. The result is that the CPA achieves instantaneous phase acquisition (0 bit) for any phase step ($\pm 2\pi$ rad). That is, no preamble bits at the beginning of the packet are necessary.

V. IMPACT OF PON SIZE ON LOCAL SOURCES VERSUS CLS PON ARCHITECTURES

In this section, we examine the relative merits (cost and performance) of local sources versus centralized architectures. The power budget of a PON is an important parameter in the design, as it helps FTTH service providers to select the appropriate light sources and the convenient receivers for their network. The power budget is mainly determined from the PON physical architecture. The uplink power budget of the CLS architecture ($P_{Budget,CLS}$) is related to that of the LS architecture ($P_{Budget,LS}$) by the following equation:

$$P_{Budget,CLS} = 10 \log \left(\frac{P_{CLS}}{P_{LS}} \right) - 10 \log N - \alpha_F D + P_{Budget,LS} \quad (3)$$

where P_{CLS} and P_{LS} are the source power for CLS and LS architectures, respectively, N is the number of splits (or number of ONUs), α_F is the fiber attenuation in decibels per kilometer, and D is the feeder length in kilometers. The first term in (3) represents the gain in relative power that can be achieved in CLS architectures; we expect P_{CLS} to be much greater than P_{LS} . The second and third terms represent the extra splitting losses and

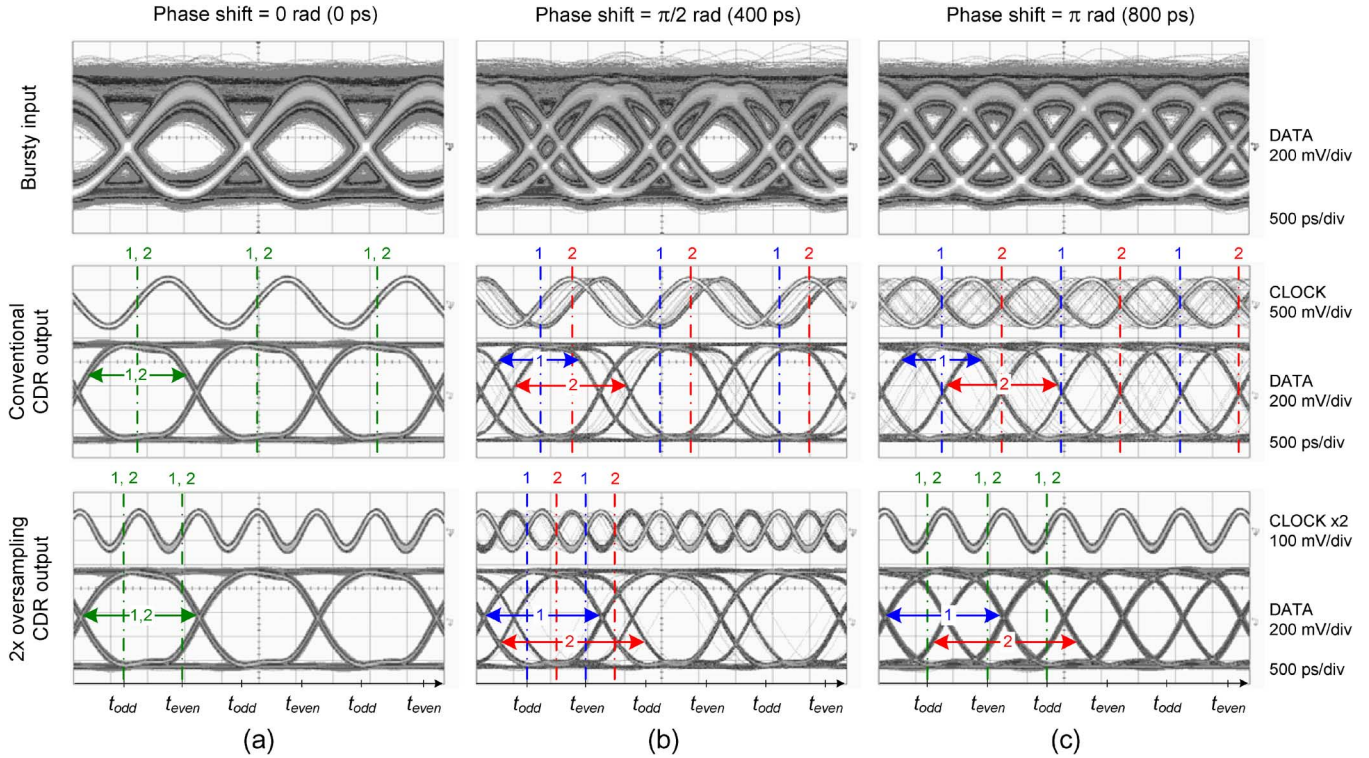


Fig. 12. Response of the CDR to bursty traffic (packets with different phases): (a) no phase difference; (b) $\pi/2$ phase difference; (c) π phase difference.

additional fiber attenuation in CLS architectures, respectively. In CLS architectures, an EDFA can be used at the central office to increase the margin by compensating the extra losses terms in (3). Using a semiconductor optical amplifier (SOA) or a reflective SOA at ONU for modulation instead of the EAM reduces the amplification requirements in both architectures [7]–[11]. Placing a gain saturated SOA at the central office can further reduce the intensity noise of BBS as in spectrum-sliced WDM PONs [24]. The possibility of integration of the external modulators (using silicon) can be advantageous from the cost point of view [25]. The selection of a powerful light source for CLS PONs also increases the power budget as in (3). The cumulative cost of light sources in LS architectures is N times the cost of a single local source, and this should be compared to the cost of the single high power source for the CLS solutions. Using powerful directly modulated LEDs at 622 Mb/s could tilt costs in favor of LS architectures by eliminating the need for modulators. However, these super luminescent LEDs have cost comparable to that of the BBS we used, and they require temperature control.

Table I details the uplink power budget and optical losses in our experimental realization of the two SAC-OCDMA PON architectures. In the column marked LS (effective), we give the values when interpreting the combination of the BBS and the first 1×8 splitter (see Fig. 3) as eight independent sources for each of the ONUs. Effectively, the total losses in the LS configuration was approximately 39 dB (excluding 9-dB losses through the $1 \times$ splitter incurred for experimental convenience), whereas the total losses in a similar CLS PON were roughly 52 dB. The 13-dB difference is the contribution of the extra 9-dB losses of the $1 \times$ coupler on the CLS first passing through RN before modulation, and the extra 4-dB losses for the unmodulated light

TABLE I
ULINK POWER BUDGET AND LINK LOSS FOR BOTH PON ARCHITECTURES

	LS	LS (Effective)	CLS
Source Power [dBm]	2.83	-6.62	2.83
RN Splitting	18.88	9.43	18.88
ODN Feeders	3.95	3.95	8.07
Loss [dB]			
Modulation	12.20	12.20	14.51
Encoding	3.99	3.99	3.99
DCF	2.41	2.41	2.41
Decoding	6.42	6.42	6.42
Total Loss	47.85	38.40	51.28
Amplification [dB]	36.56	36.56	40.84
Received Power [dBm]	-8.46	-8.46	-7.61

traversing 20 km of SMF. For our experiment, examining the final two columns of Table I, $P_{\text{Budget,CLS}} = -48.45$ dBm (excluding amplification), $P_{\text{Budget,LS}} = -45.02$ dBm (excluding amplification). Note that $P_{\text{CLS}}/P_{\text{LS}}$ was chosen to offset the RN losses of $10 \log N$ dB, so the only remaining difference was the additional fiber losses.

The second 8×1 coupler in Fig. 1(a) represents the splitting loss at the RN. From Table I, the RN splitting losses represent the major source of losses, and would be higher for larger PONs with $1:32$ or $1:64$ splitting ratio. Fiber losses are the combinations of propagation losses (20 and 40 km of SMF-28 for LS and CLS architectures, respectively), and a 2.41-dB loss DCF. The modulation losses for the CLS PON are greater than those of the local sources, as the input power to the modulator is lower (see Fig. 3); the light travels a 20-km feeder before it reaches the ONU. Encoding and decoding losses are related to the design of

the codes and FBGs, namely, the code weight and the reflectivity of each frequency bin. The decoding losses shown in Table I include also a 3.5-dB loss of the 1×2 coupler at the balanced receiver. Modulation and encoding/decoding losses should remain almost the same for larger PONs. Because the EDFAs are not gain clamped, we note that the gain varies from one configuration to the other depending on the corresponding EDFA input power. The maximum received power levels for both architectures are illustrated in Table I; recall that at -23 dBm we achieve error free operation for the two PON architectures. Practically, the gain of the EDFAs, as well as the source power, must be sufficient to overcome the losses and the limited sensitivity of the receiver. Using avalanche photodetectors (APD), for example, increases the link margin.

Extrapolating our results for larger PONs using (3), we note that in CLS architectures the loss budget goes up with the square of the number of splits, instead of being proportional to the number of splits for the LS solution. In other words, doubling the number of users in an LS architecture imposes an additional 3-dB loss, whereas for CLS PONs there is a 6-dB extra loss. The same relationship holds when increasing the PON physical reach. However, as discussed earlier, this extra loss can be compensated using amplification at the OLT, or SOAs at the ONUs, without increasing the cost significantly.

VI. SUMMARY AND CONCLUSION

We proposed and experimentally demonstrated different incoherent SAC-OCDMA PON physical architectures using a standalone burst-mode receiver at the OLT side. Local sources and centralized sources architectures have been examined. For experimental convenience, we examined only the two-feeder architecture; therefore, the effects of Rayleigh backscattering are not addressed. Continuous and bursty upstream traffic for seven asynchronous users at 622 Mb/s were considered for the BER and the PLR measurements, respectively. We performed measurements at a bit rate of 666.43 Mb/s when using FEC to account for its overhead. Furthermore, we analyzed the power budget and the relative merits of LS versus CLS architectures. A small penalty of 2 dB added to the CLS with respect to the LS architecture was measured at a BER of 10^{-9} . We presented a simple power budget equation relating CLS to LS architectures. Using that equation, we can extrapolate our results to larger SAC-OCDMA PONs. We showed that CLS architectures experience double the ODN and RN losses of similar LS PONs, whether the two-feeder or single-feeder topology is used. Doubling the number of users imposes an additional 3-dB loss in LS architectures, whereas doing the same for CLS architectures imposes an extra 6-dB loss. CLS architectures can overcome these penalties using amplification at the central office, or even SOAs at the ONUs for modulation. Alternately, central office amplification can be used to more than double the number of users in LS SAC-OCDMA PONs. The selection of appropriate light sources for both architectures also plays an important role in the power budget, and can help increase the link margin.

The OLT receiver we designed features automatic detection of payload, clock-and-data recovery, instantaneous (0 preamble bit) phase acquisition for any phase step, and FEC with a

RS(255, 239) decoder. Furthermore, the receiver significantly reduced the intensity noise of the BBS, and other impairments, by quantizing (refer to the output of the CDR in Fig. 12). We have also shown that the penalty added by the global clock due to the nonideal sampling is negligible. Error-free transmission (uplink) was achieved for a fully loaded system of seven users for LS and CLS architectures. A coding gain of more than 2.5 dB at $\text{BER} = 10^{-9}$ was reported and BER floors for five users (only for the CLS PON) and seven users were eliminated with FEC. The FEC had one order of magnitude worse performance than that predicted for a memoryless channel.

When using the CPA, we have reported a zero PLR for up to four simultaneous users (for any phase difference between packets), and more than two orders of magnitude improvement for a fully loaded system (compared to using only the CDR without CPA) for the worst phase shift between packets. Our burst-mode SAC-OCDMA receiver proved to have a good immunity to silence periods in the sense that it can support several hundreds of CIDs at 622 Mb/s; therefore, it is suitable for PON applications because the standards restrict the maximum CIDs to only 72 bits [21], [22].

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