A 3.125-Gbit/s Parallel Optical Receiver in 0.13-μm CMOS With Direct Crosstalk Power Penalty Measurement Capability

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***Abstract*—We introduce a new method to measure the crosstalk power penalty in an arrayed environment by using an on-chip pseudorandom-bit-sequence generator to drive the aggressors. The proposed method is implemented in a three-channel 3.125-Gbit/s/ch parallel receiver. Experimental results are presented including measurements of bit-error rate and crosstalk power penalty for 2.5- and 3.125-Gbit/s operations. The measured crosstalk power penalty is less than 1 dB at both data rates. The test chip was designed in a standard 0.13-μm CMOS process.**

***Index Terms*—Crosstalk, parallel optical interconnects (POI), transimpedance amplifier (TIA), truly differential, 0.13-μm CMOS.**

I. Introduction

PARALLEL optical interconnects (POI) are an efficient way to increase the aggregate bandwidth for very short reach (VSR) applications [1]–[3]. A low-power 10-Gbit/s receiver front-end has been reported [4]; and a terabit optical bus was demonstrated for chip-to-chip communications in high-end servers [5]. More recently, Pappu *et al.* [6] have proven that even for very short on-chip distances, optically interconnected systems will have a lower energy-delay-squared product $(\mathrm{E}\tau^2)$ than electrical interconnects when the fan out number increases. Further investigation of CMOS-based transceivers for VSR optical interconnects is both necessary and promising.

Most of the commercial parallel transceiver modules have a channel separation of 125 or 250 μm to be compatible with the channel pitches of the ribbon fibers, vertical cavity surface emitting laser (VCSEL) arrays, and photodiode (PD) arrays. The electrical crosstalk issue becomes more critical as on-chip clock frequencies continue to increase and more analog and digital blocks are integrated on the same die to realize system-on-chip (SoC) capability. It is widely accepted that the major sources of crosstalk are substrate coupling from neighbors, coupling between bondwires, and switching noise coupled from the supply rails [7]. To alleviate the effects of crosstalk on signal integrity at high data rates, several common design guidelines have been used in previous work to improve crosstalk isolation, such as separate supply lines for analog and digital blocks, increased number of ground connections, deep-N-wells and guard rings to protect sensitive circuits from substrate couplings, select high-resistive P-substrate process, on-chip or flip-chip decoupling capacitors [8], etc.

To quantitatively characterize receiver immunity to crosstalk, the crosstalk power penalty is often measured as an important figure of merit in addition to the crosstalk transfer characteristic. However, it is not easy to emulate a realistic working environment to accurately measure the crosstalk power penalty before the chip is put into the field. A multichannel parallel pattern generator is most suitable for the requirements but is an expensive piece of equipment. In an alternate approach, Schild *et al.* [9] adopted a cost-effective solution to characterize the crosstalk effect. One pseudorandom-bit-sequence (PRBS) signal is split into three channels to drive both the dummy channels and the channel under test. The drawback of this method is that all dummy channels in the same block are switching at the same time because they are sharing the signal source. Since the data rates of the aggressor and the victim are also the same, the added switching noise peaks always appear at fixed positions in time. Therefore, the crosstalk test results using this method are of a pessimistic nature.

We report a new method to measure the crosstalk power penalty accurately in an arrayed environment. An on-chip PRBS generator is implemented to drive the aggressors adjacent to the victim. This new method has three advantages.

1) No expensive multichannel signal source is required.
2) The data rate and pattern of the dummy channels are independent of channel under test. This more accurately emulates a realistic working environment.
3) No high-quality PRBS generator and clock generator are needed, hence the design effort to integrate the test circuitry on chip is reduced.

The proposed idea has been implemented with a three-channel, truly differential optical receiver in 0.13-μm CMOS. The proposed receiver front-end runs error free at 3.125 Gbit/s with -16-dBm sensitivity and 22-mW channel power consumption. The differential output swing is 400-mV peak-to-peak over 50-Ω loads. On-chip ac coupling capacitors are used to convert a pseudodifferential signal into a truly differential signal by removing the dc components from the transimpedance amplifier (TIA) output. This step is necessary before integrating digital circuitry with the receiver front-end for post processing since pseudodifferential signals make the choice of decision threshold difficult [10].

This paper is organized as follows. The design and implementation of the crosstalk power penalty measurement method and

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the receiver structure are described in Section II. Experimental results are presented in Section III and concluding comments are given in Section IV.

II. Circuits Design

A. Crosstalk Power Penalty

When it comes to measuring the crosstalk power penalty in parallel receiver testing, the designer faces the problem of how to drive the aggressors with the most realistic working conditions. A commercial multichannel parallel test system running at 10 or 40 Gbit/s can be costly. Instead, a cost-effective solution is presented in [11], which integrates 12 commercial 10 Gigabit Ethernet physical layer integrated circuits (ICs) in a customized testing station. Each aggressor is driven by a PRBS signal generated by the physical layer IC with independent data rates and patterns. This method is very flexible as each transceiver channel can be controlled independently, both in optical modulation amplitude and line rates, to serve different testing purposes. Therefore, it represents a realistic working environment, although the effort for customized integration of the 12 10 G Ethernet ICs is nontrivial.

Another simple solution to measure the crosstalk power penalty is to power-split one PRBS signal source and use it to drive both the aggressors and the channel under test [9] as mentioned in Section I. Because a single PRBS source is used, the data rate and data pattern of the aggressors and the victim are identical. The phase relationship between the aggressors and the victim are fixed (delayed by several bits). Therefore, all the aggressors in each block are switching at the same time. The added switching noise peak is always presented to the victim after a fixed delay time. The relative positions of these noise peaks in the eye opening are critical for accurate bit-error-rate (BER) measurements. For example, if the noise peak appears at the crossing point in the eye diagram while the decision circuit is sampling the data in the middle of the eye, the effect of the crosstalk is underestimated. On the other hand, if the noise peak appears in the sampling window of the eye diagram, the effect of crosstalk tends to be overestimated. The phase difference between the aggressors and the victim cannot be accurately controlled over the fixed delay stubs on-chip.

In order to achieve higher accuracies, we introduce a new method to measure the crosstalk power penalty in an arrayed environment, as shown in Fig. 1. To analyze crosstalk, three identical receiver channels are implemented side by side with a 250-μm separation. Only the middle channel will be tested. An on-chip PRBS generator is used to drive the dummy channels through a scaled PD emulator (PDE) that is similar to the one used in [12]. The BER measurements also employ an on-chip PDE. The data rate of the PRBS generator can be fine-tuned by adjusting the oscillating frequency of the voltage-controlled oscillator (VCO), thus it is independent of the channel under test and therefore reflects a realistic working environment. Both aggressors still switch at the same time although they are independent of the channel under test. However, since the data rate of the dummy channels is slightly different from the channel under test, the noise peaks are randomly distributed as seen by the victim.

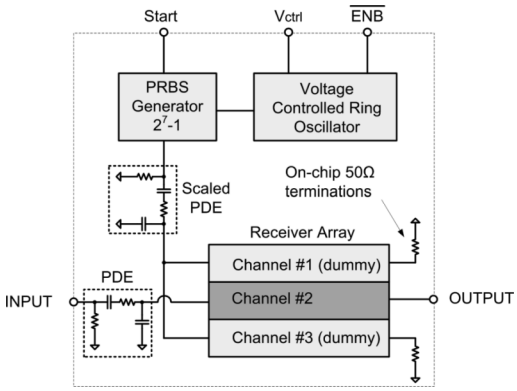

Fig. 1. Block diagram of the parallel optical receiver chip with on-chip clock and PRBS generators for crosstalk power penalty measurement.

The proposed method is convenient for parallel testing because no high-quality PRBS generator is needed; in addition the design effort and layout overhead are kept to a minimum. The PRBS generator and the VCO use different on-chip power supply networks, and thus can be turned off completely to minimize unnecessary power dissipation and noise. The PRBS generator is based on shift registers and can generate a pattern length of 2^7–1. The VCO is a single-ended ring oscillator based on current-starved inverters.

Optical crosstalk is not considered in this work for two reasons: 1) the parallel receiver is not designed to work with wavelength division multiplexing (WDM) devices in which the imperfection of the multiplexer and demultiplexer incurs most of the optical crosstalk; 2) the state-of-art monolithic PDs have an active area diameter less than 50 μm which is comparable to the core size of a 50/125 or 65/125 multimode fiber. The cleaved fiber-end is butt-coupled to the PD. Considering the PD pitch is 250 μm, the optical crosstalk at the receiver input is negligible.

B. Receiver Architecture

The block diagram of one channel of the front-end circuits is illustrated in Fig. 2(a). It is composed of a TIA, an input buffer (IB), a limiting amplifier (LA), and a current-mode-logic (CML) buffer. The IB, LA, and CML buffer are referred as the post-amplifier. One end of the differential input port of the TIA is wire bonded to a PD or a PDE for testing purposes, while the other end is connected to a dummy capacitor through a bond wire for balance. The dummy capacitor is matched to the PD parasitic capacitance. To alleviate the effects of any common-mode noise coming from the supply rails and substrate, every stage of the receiver follows a fully balanced differential structure. The size of R_F and $C_{\rm PD}$ are 1 kΩ and 0.4 pF, respectively. The PD parasitic capacitance was measured from the available 1 $\times$ 12-PD array [13]. The simulated TIA low cutoff, high cutoff frequencies, and the differential transimpedance gain are 180 kHz, 2.6 GHz, and 56.2 dBΩ, respectively.

Due to the single-ended nature of the PD, the output of the TIA is a pseudodifferential signal. The major difference between a pseudo and a truly differential signal is the dc component. For a pseudodifferential signal, the dc components of $\rm data$ and $\overline{\rm data}$ have a large offset which makes the choice of the decision threshold difficult [10]. By ac coupling the TIA outputs to the

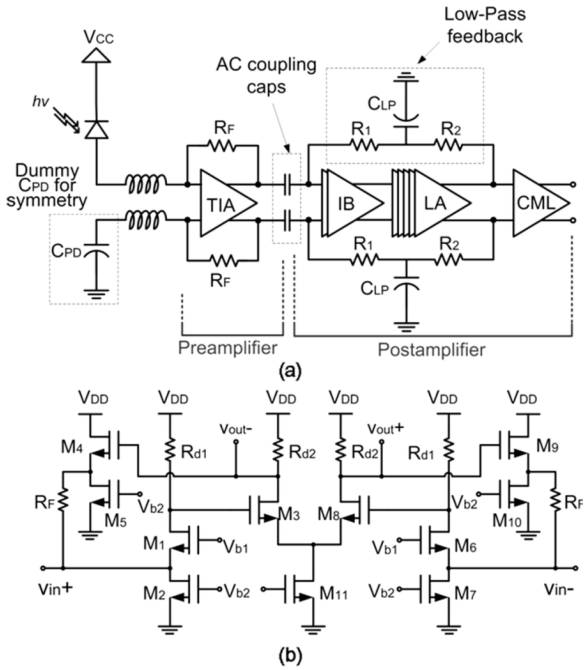

Fig. 2. (a) Block diagrams of one receiver channel; (b) TIA schematics.

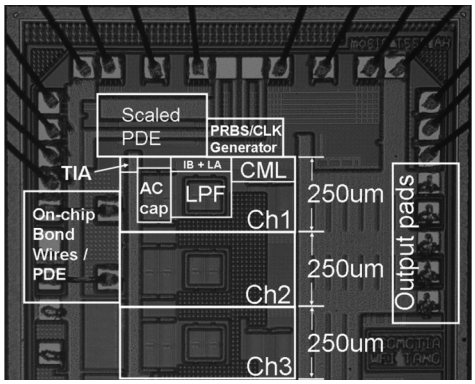

Fig. 3. Micrograph of a wireboded die sample.

post-amplifier, the dc components are blocked hence the output is converted to be truly differential. However, the output voltage will drop due to the limited low cutoff frequency for input data patterns with long consecutive identical digits (CID). This introduces pattern-dependent-jitter (PDJ) into the system [14]. The size of the coupling capacitors was chosen according to the analysis presented in [14] to minimize the effect of the PDJ. The total resistance seen by the capacitor is large $(> 10\,\mathrm{k}\Omega)$ since it is connected between two high-impedance nodes. Therefore, it is possible to design a circuit using capacitors that are small ($\sim$10's pF) and can be built on-chip. We choose the capacitor size to be 20.5 pF so that the introduced PDJ is less than 2 ps (calculated) with PRBS $2^{23} - 1$. The capacitors are implemented as dual metal-insulator-metal (DMIM) capacitors and occupy an area of $180\,\mu\mathrm{m} \times 110\,\mu\mathrm{m}$ as shown in Fig. 3.

Traditional dc-offset cancellation techniques can also be used to perform the pseudodifferential to truly differential conversion [15]. Two matched operational transconductance amplifiers (OTA) are needed in addition to two 18-pF capacitors for the differential conversion. The size of the capacitors used in [15] is similar to this work, but the OTAs require more design effort and consume more power compared to the ac coupling technique presented here, which uses only capacitors.

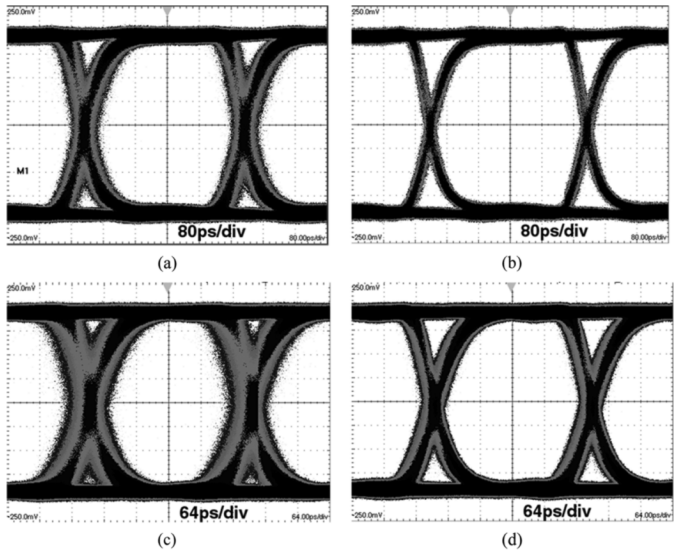

Fig. 4. Measured differential eye diagrams at 2.5 and 3.125 Gbit/s with single-channel operation. (Vertical: 50 mV/div). (a) 2.5 Gbit/s, 20 μA input. (b) 2.5 Gbit/s, 220 μA input. (c) 3.125 Gbit/s, 20 μA input. (d) 3.125 Gbit/s, 220 μA input.

TABLE I
MEASURED RMS JITTER FOR DIFFERENT INPUTS

	(Gbit/s)	Input (μA)	RMS Jitter (ps)		
			PRBS 2^7-1	PRBS 2^{15}-1	PRBS 2^{23}-1
Non disturbed	2.5	20	9.8	12.7	12.8
		220	5.4	6.4	6.6
	3.125	20	13.4	14.9	15
		220	8.1	8.5	8.7
Disturbed	2.5	20	12.3	14.4	14.6
		220	5.7	6.5	6.9
	3.125	20	16.5	18.0	18.3
		220	8.9	9.2	9.4

III. EXPERIMENTAL RESULTS

This chip is fabricated in the IBM CMRF8SF-DM process which uses a lightly doped P-substrate. Blank chip area is used for decoupling capacitors to eliminate the switching noise on the supply network. Deep-N-wells and P+ guard rings are used to shield sensitive circuit blocks from substrate coupling. The bare die is wire-bonded to an 80-pin ceramic-flat-pack (CFP) package, clamped to a general purpose RF test fixture. Two RF probes are used to apply/collect the input/output signals directly at the die to eliminate the effect of package parasitics.

Measured differential eye diagrams at 2.5 and 3.125 Gbit/s for different input levels are shown in Fig. 4. The test PRBS sequence length is $2^{23} - 1$. Clear open eyes are observed for the input photon current range from 20 to 220 μA with a constant $400\mathrm{mV_{pp}}$ output swing. Due to the ac coupling capacitors used between stages, PDJ is observed. The rms jitter is 15 ps at 3.125 Gbit/s and 12.8 ps at 2.5 Gbit/s for 20-μA input. Details of rms jitter measurement results for different input levels are shown in Table I. The rms jitter increases with the input PRBS sequence length due to the PDJ introduced by ac coupling capacitors.

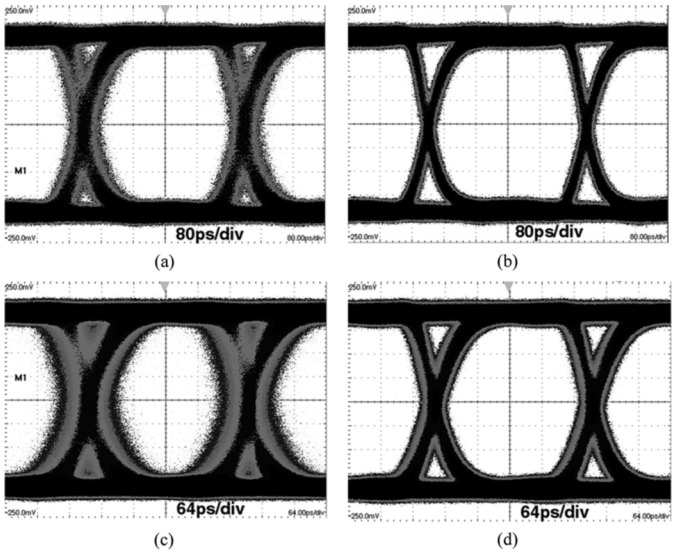

Fig. 5. Measured differential eye diagrams at 2.5 and 3.125 Gbit/s with adjacent channels turned on. (Vertical: 50 mV/div). (a) 2.5 Gbit/s, 20 μA input. (b) 2.5 Gbit/s, 220 μA input. (c) 3.125 Gbit/s, 20 μA input. (d) 3.125 Gbit/s, 220 μA input.

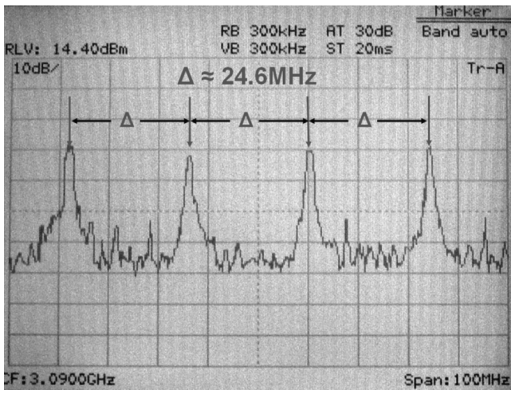

Fig. 6. Output spectrum of the PRBS generator. The separation of the peaks is the clock frequency divided by the PRBS sequence length.

The middle channel suffers from the crosstalk induced by the neighboring channels when the on-chip PRBS generator is turned on. The differential eye diagrams are shown in Fig. 5. Compared with the single-channel operation eye diagrams in Fig. 4, the eye openings are slightly decreased due the increased noise power on the low/high rails. The rms jitter is also much higher than single-channel measurement results as shown in Table I.

The frequency spectrum of the PRBS generator output is shown in Fig. 6. The separation of the peaks is approximately 24.6 MHz. This spectrum proves that the PRBS pattern length is $2^7 - 1$ as shown

$$\Delta = \frac{3.125\ \text{Gbit/s}}{2^7 - 1} \approx 24.6\ \text{MHz}. \tag{1}$$

Fig. 7 depicts the single-ended BER measurement results. The equivalent input optical power is calculated based on the simulated PDE voltage-current conversion efficiency, which is 110 $\mu\text{A}/\text{V}$. And also a PD responsivity of 0.8 A/W is assumed to perform the calculation.

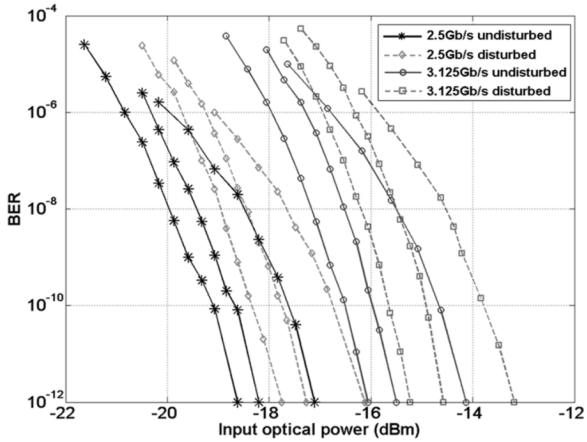

Fig. 7. Single-ended BER measurement results for 2.5 and 3.125 Gbit/s. Each group contains 3 BER curves which correspond to 3 different PRBS sequence lengths. From left to right: PRBS 2^7–1, PRBS 2^{15}–1, and PRBS 2^{23}–1.

TABLE II
MEASURED CROSSTALK POWER PENALTY FOR DIFFERENT PRBS LENGTHS

	PRBS 2^7-1	PRBS 2^{15}-1	PRBS 2^{23}-1
2.5Gbit/s	0.87-dB	0.93-dB	0.99-dB
3.125Gbit/s	0.83-dB	0.92-dB	0.95-dB

TABLE III
COMPARISON OF CROSSTALK POWER PENALTY WITH PREVIOUS WORKS

	[16]	[17]	This work	[18]	[11]	[8]
Technology	HBT	SiGe BiCMOS	130nm CMOS	SiGe BiCMOS	0.35μm SiGe	InGaP/ GaAs HBT
Data rate (Gbit/s)	2.5	2.488	3.125	8.5	10	10
Crosstalk power penalty (dB)	<1	<0.4	<1	<1.3	<3.5	0.8

Anritsu 12.5-Gbit/s pattern generator MP1763B and error detector MP1764A are used to test the BER. The BER performances are tested with three different PRBS sequence lengths, 2^7–1, 2^{15}–1, and 2^{23}–1. With PRBS length 2^7–1, the sensitivity is -16 dBm at 3.125 Gbit/s $(\text{BER} < 10^{-12})$ for single-channel operation. At 2.5 Gbit/s, the sensitivity is -18.7 dBm. When tested with PRBS length $2^{23}-1$, the sensitivities increase to -14.2 dBm and -17.2 dBm for 3.125 and 2.5 Gbit/s, respectively. The increase of sensitivity is attributed to the PDJ as a result of ac coupling capacitors used between the stages. The crosstalk power penalty falls between 0.83∼0.99 dB for both 2.5 and 3.125 Gbit/s as calculated from the waterfall curves in Fig. 7. Detailed results are summarized in Table II.

Table III gives a comparison of the crosstalk power penalty with previous published work. These measurement results are comparable with other parallel receivers fabricated in different technologies.

The measured channel power consumption is 22 mW with a 400-mV peak-to-peak differential output swing. The 3-stage tapered CML buffer dissipates 13.8 mW while the TIA draws approximately 2.1-mA current from a 1.2-V supply. The channel power dissipation is reduced to 9.3 mW if we decrease the power supply of the post-amplifier to 0.75 V with only 100mV_{pp} differential output amplitude. The reduced amplitude differential eye diagrams for 2.5 and 3.125 Gbit/s are shown in

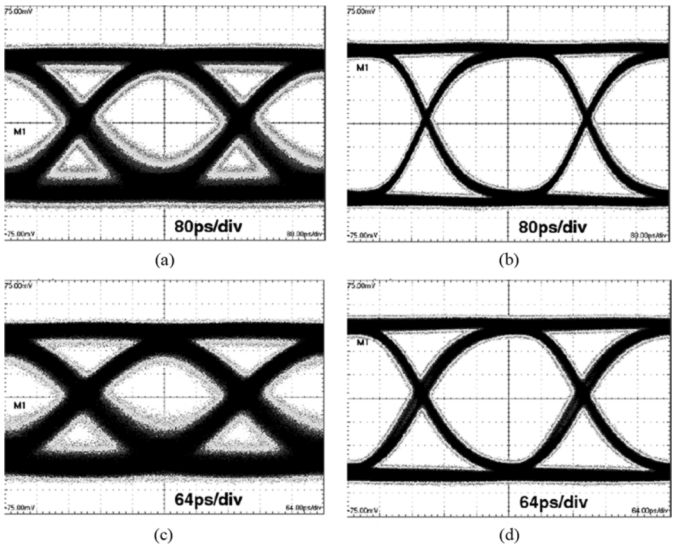

Fig. 8. Measured differential eye diagrams with 0.75-V supply for the post amplifier. (vertical: 15 mV/div). (a) 2.5 Gbit/s, 20 μA input. (b) 2.5 Gbit/s, 220 μA input. (c) 3.125 Gbit/s, 20 μA input. (d) 3.125 Gbit/s, 220 μA input.

Fig. 8. BER was measured with the help of an external RF amplifier HP8347A. Error free operation is achieved at -16 dBm (-14.6 dBm) for 2.5 Gbit/s (3.125 Gbit/s). We estimate the power could still be decreased to less than 6.5 mW considering less gain stages are needed for reduced voltage swing.

IV. Conclusion

As the CMOS technology scales to deeply sub-micron dimensions, the peak unity-gain frequency of nMOS transistors rises above 100 GHz, which makes CMOS processes very attractive for implementing high frequency circuits. However, channel crosstalk will be one of the major limiting factors in future parallel transceiver designs. Accurately measured crosstalk power penalty is necessary when calculating the link budget.

We have presented a new method to measure the crosstalk power penalty accurately in an arrayed environment by using on-chip PRBS generator to drive the aggressors. A three-channel parallel optical receiver was implemented to evaluate the proposed method. The measured crosstalk power penalty is less than 1 dB at 2.5 and 3.125 Gbit/s, which is comparable with previous work in different technologies.

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