Burst-Mode Clock and Data Recovery in Optical Multiaccess Networks Using Broad-Band PLLs

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***Abstract*—Broad-band phase-locked loops (PLLs) are proposed for burst-mode clock and data recovery in optical multiaccess networks. Design parameters for a charge-pump PLL-based clock and data recovery (CDR) with fast phase acquisition are derived using a time-domain model that does not assume narrow loop bandwidth or small phase errors. Implementation in a half-rate CDR circuit confirms a clock phase acquisition time of 40 ns, or 100 bits at 2.488-Gb/s rate, and data recovery at 1.244-Gb/s rate with a bit-error rate of 1×10^{-10} ($2^{14} - 1$ pseudorandom binary sequence with Manchester-encoding). The CDR was fabricated in complementary metal–oxide–semiconductor 0.18-μm technology in an area of 1×1 mm^2 and consumes 54 mW of power from a 1.8-V supply.**

***Index Terms*—Burst-mode receivers, clock and data recovery (CDR), half-rate clock and data recovery (CDR), multiaccess communication, optical communication, phase-locked loops (PLLs).**

I. Introduction

DEMANDS for broad-band access are predicted to exceed the potential of modern networks. Optical multiaccess networks based on an all-optical core, such as passive optical network, have been proposed to enable services such as IP telephony and video on demand in metro and access areas [1], [2]. Technologies focusing on this all-optical core are already mature [3]. However, novel electronics are also required to support new functionalities at the network edges. Specifically, optical receivers must be adapted to deal with burst-mode traffic, where data bursts originate from various sources and travel different distances due to the point-to-multipoint nature of the network. The amplitude and phase of successive packets may therefore vary anywhere between 0–20 dB and $-\pi$ to $+\pi$ rad, respectively [4]. Receivers with the following characteristics are therefore necessary: wide dynamic range, fast automatic threshold control (ATC), and fast phase acquisition, where ATC and phase acquisition must occur within nanoseconds to support short packet lengths at gigabit rates. Burst-mode receiver front-ends have already been demonstrated with wide dynamic range and fast ATC [5]. This work focuses on the fast phase acquisition requirement. Whereas previous works have considered correlation algorithms [6] and gated oscillators [7] to decrease phase acquisition time in clock and data recovery (CDR), this work investigates the use of broad-band phase-locked loops (PLLs). While it is known that increasing the bandwidth of a PLL can tradeoff jitter performance in favor of phase/frequency acquisition time [8], this work addresses practical issues in applying this concept to burst-mode CDR. We demonstrate successful implementation of a burst-mode broad-band PLL CDR through modeling and experimentation, and quantify the resulting tradeoff on line coding. In particular, the phase acquisition time of a broad-band PLL CDR is measured and the effect of various coding schemes on the phase noise of the recovered clock is tested. Section II discusses the advantages and tradeoffs of broad-band PLL CDRs. Section III describes modeling and implementation, while Section IV describes the experimental results.

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II. Broad-Band PLL CDR

SONET CDRs are specified with a narrow PLL bandwidth in order to minimize jitter accumulation through long repeater chains in long-haul networks [9]. This is because narrow-band PLLs are highly resistant to phase variations which cause jitter. However, this optimizes SONET CDRs for suppression of data jitter at the expense of other abilities: suppression of internal jitter from the voltage-controlled oscillator (VCO), frequency capture range, and phase/frequency acquisition time. This last tradeoff is central to the discussion. A narrow-band PLL's resistance to phase variations implies a slow acquisition time to steps in the incoming phase. The phase acquisition time of a commercially available SONET OC-48 CDR was previously measured at 1400 bits ($\pm\pi$-rad phase steps) [10], which translates to microseconds at gigabit rates. In contrast to SONET networks, optical multiaccess networks are typically deployed in metropolitan areas where few or no repeaters are necessary. This opens the possibility of relaxing the restriction on the PLL's loop bandwidth.

We therefore consider a broad-band PLL CDR to achieve fast phase acquisition in optical multiaccess networks. Specifically, we modify the PLL parameters in a SONET CDR to increase loop bandwidth until a target phase acquisition time is obtained. Theoretically, this has the added benefits of increasing the CDR's frequency capture range and suppression of internal jitter, as the PLL behaves as a high-pass filter for jitter generated by the VCO [8]. However, as PLLs are unable to distinguish a true phase-step from cycle-to-cycle data jitter, increasing the loop bandwidth simultaneously increases the jitter transfer bandwidth. Also, broad-band PLLs are more prone to clock drift when receiving data with low transition-density, making line coding necessary to eliminate low frequency components. Therefore, the tradeoffs are reduced suppression of data jitter and a strong requirement for line coding. We quantify these tradeoffs below.

III. Modeling and Implementation

Although they are of higher order and complexity, charge-pump PLL-based CDRs are often simplified to second-order

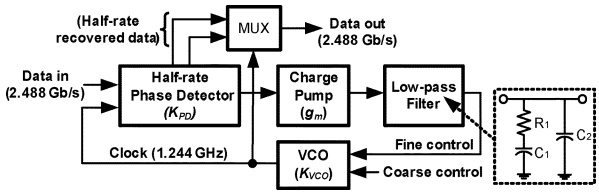

Fig. 1. Half-rate CDR architecture [11], targeting a 2.488-Gb/s bit rate.

models used in the frequency-domain. However, their accuracy relies heavily upon two assumptions [11]: 1) the instantaneous phase error (φ_e) between the input and the recovered clock is small, which restricts the model to cases where the system does not deviate far from steady-state; and 2) the loop bandwidth (K) is a small fraction of the input frequency ($\gg 10 \cdot K$ [11]), which allows a continuous-time approximation of the loop's behavior where digital switching granularity is ignored in favor of the average behavior over many cycles. The two assumptions produce a linear baseband model of charge-pump PLLs to facilitate analysis. However, these assumptions do not apply in the present case. Another consideration is that stability becomes an issue as a PLL's bandwidth is increased. This is especially true for charge-pump PLLs, which are time-variant due to the discontinuous sampling operation [11]. A more reliable model is therefore necessary for this application, particularly when modeling responses to large phase steps.

An alternative mathematical model for charge-pump PLLs was proposed in [11] and [12]. The model is based on a system of nonlinear difference equations that account for the highly nonlinear nature of PLLs directly in the time-domain. It therefore places no restrictions on K or φ_e to produce transient responses to phase steps. The model was used here to derive component values which achieve fast phase acquisition in a half-rate CDR architecture intended for SONET [8] (Fig. 1). Specifically, parameters for a second-order loop filter $(R_1, C_1, C_2,)$ and linear gains for the phase detector (K_{PD} [V/rad]), charge-pump (g_m [A/V]), and VCO (K_{VCO} [Hz/V]) were derived for a target clock frequency of 1.244 GHz (Table I). Fig. 2 shows the resulting transient responses (VCO control voltage) to phase steps within the range $[0, \pm\pi/2]$ rad, which were generated using the model. Note that the input is a periodic signal resembling a burst preamble and that frequency-lock is assumed as an initial condition. Stability is verified over all simulated phase steps. In all cases, the CDR requires 40 ns to settle to within approximately 10% of the steady-state value, corresponding to 100 bits at 2.488-Gb/s data rate. In comparison, [8] exhibited a 350-ns lock time. To quantify the jitter tradeoff, the analysis and equations from [8, Ch. 5] were used to derive the loop bandwidth and jitter peaking resulting from the design parameters of Table I. K was calculated to be 5.78×10^8 rad/s, or 92 MHz, while jitter peaking was 1.202 dB. These results denote a wider jitter transfer bandwidth and higher peaking than specified in ITU/Bellcore specifications for SONET OC-48 (2 MHz and 0.1 dB, respectively [9]). This confirms that a broad-band PLL CDR has been achieved resulting in a tradeoff in data jitter-suppression abilities. Also, the ratio of clock frequency over K is only $\sim$13.5, indicating that performance assessments from a baseband frequency-domain model would not be reliable [11].

The derived PLL parameters were implemented in the CDR architecture from [8], targeting a data rate of 2.488 Gb/s. The

TABLE I
CIRCUIT DESIGN PARAMETERS OBTAINED FROM SIMULATION

Parameter	Value
R_1	5 KΩ
C_1, C_2	2.5 pF, 300 fF
K_{PD}	25 mV/rad
g_m	400 μA/V
K_{VCO}	2.0 GHz/V
$I_P (= K_{PD} \cdot g_m)$	10 μA/rad

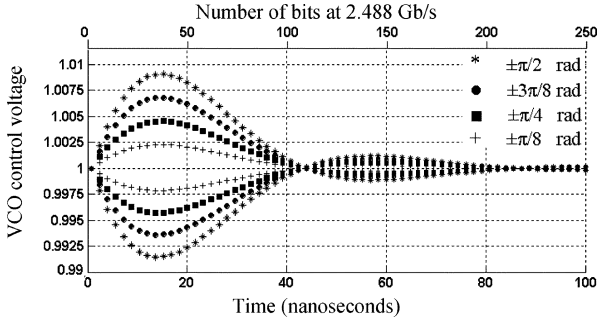

Fig. 2. Transient simulation from nonlinear time-domain model of VCO control voltage with respect to time and number of bits of incoming data (2.488 Gb/s) in response to phase steps of $\pm\pi/8$, $\pm\pi/4$, $\pm 3\pi/8$, and $\pm\pi/2$ rad.

architecture is a half-rate CDR which samples data on both the rising and falling edges of the clock. Such architectures use a VCO running at half the data rate to facilitate implementation in complementary metal–oxide–semiconductor (CMOS), and offer significant advantages in the proposed application. Following a phase step, the worst-case clock realignment is $\pm\pi/2$ rad, as opposed to $\pm\pi$ rad for a full-rate architecture. Also, each recovered bit occurring on the negative-edge of the clock would not be sampled by subsequent positive-edge triggered systems. Therefore, in the case of Manchester-encoded data, this would automatically recover the original uncoded data if made to positively trigger on the correct cycle of bits.

The phase detector was implemented using CML logic to reduce switching noise and increase speed. The gains of the implemented phase detector, charge-pump, and VCO were 23.56 mV/rad, 395 μA/V, and 1.93 GHz/V, respectively. In order to observe phase acquisition, the differential control voltage of the VCO was brought off-chip using a buffer, to minimize loading effects, and an amplifier. This added significant power consumption but enabled observation of the internal PLL behavior during transients. Fifty-Ohm low-voltage differential signal input–output buffers were used to bring high-speed signals on- and off-chip.

IV. EXPERIMENTAL RESULTS

The circuit was fabricated in CMOS 0.18-μm in an area of 1×1 mm^2. The die was packaged in a 24-pin open-cavity ceramic package mounted on a custom designed FR4 printed circuit board. The measured power consumption was 54 mW from a 1.8-V power supply. The VCO could operate anywhere between 622 MHz and 1.244 GHz using coarse tuning.

The phase acquisition time of the CDR was measured using a repeating 2.488-Gb/s pattern consisting of 32 consecutive zeros, representing a period of nontransmission, followed by a 112-bit "1010..." pattern, representing the preamble of a burst packet.

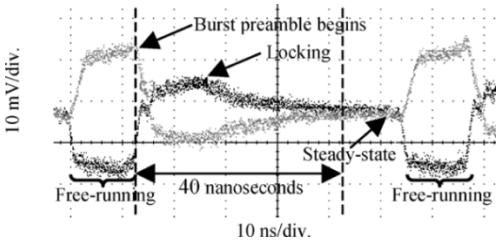

Fig. 3. Scope trace of differential VCO control signal from implemented circuit in response to data burst preamble.

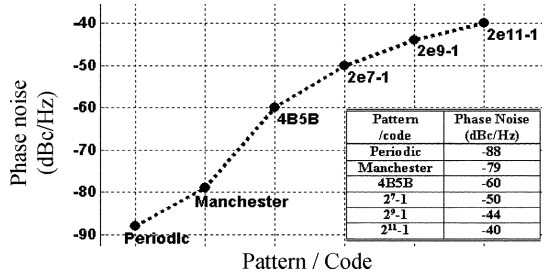

Fig. 4. Phase noise measured at 1-MHz offset from peak for various data patterns of decreasing transition density.

Fig. 3 depicts a scope trace of the PLL's response (VCO control voltage). Note that the trace is an amplified version of the control voltage. The periods of nontransmission and preamble are each evident in the trend. During periods of nontransmission, the system is free-running and the phase of the VCO is random with respect to incoming data. The CDR begins locking at the beginning of the preamble and reaches steady-state within approximately 40 ns, or 100 bits at 2.488 Gb/s. The trend and timescale of the CDR response are comparable to simulation results (Fig. 2), which verifies the accuracy of the PLL model proposed in [10]. It also confirms that a greater than ten-fold improvement in phase acquisition time has been achieved over that of a SONET CDR [10].

The CDR was then tested with various line coding schemes. As expected, a strong dependence on transition density was observed (Fig. 4). Only Manchester-encoding resulted in a recovered clock of sufficient quality for bit-error-rate (BER) testing. Manchester-encoded pseudorandom binary sequence patterns of length 2^7-1, $2^{11}-1$, and $2^{14}-1$ were used to make BER measurements. Error-free data recovery could not be achieved at 2.488 Gb/s due to poor performance of the data output buffers, which resulted in attenuation. The CDR was therefore tested at 1.244 Gb/s with a recovered half-rate clock of 622 MHz. This produced a baud rate of 1.244 Gb/s and an effective recovered bit rate of 622 Mb/s due to Manchester-encoding. BER measurements were performed by loading Manchester-encoded patterns into the pattern generator and the corresponding uncoded patterns into the error detector. This resulted in a BER of 1×10^{-10} for all three patterns. Fig. 5 depicts a persistence scope trace of the recovered data. The small vertical eye opening (50 mV) is caused by attenuation by the data output buffers. Fig. 6 depicts the recovered clock spectrum for a Manchester-encoded pattern. A phase noise of -79 dBc/Hz was measured at a 1-MHz offset.

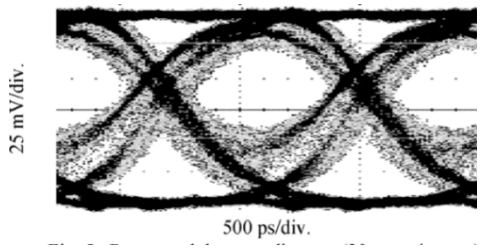

Fig. 5. Recovered data eye diagram (20 s persistence).

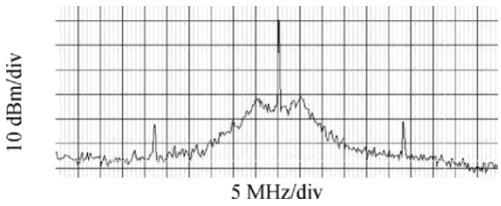

Fig. 6. Spectrum of recovered clock, 100-MHz span (peak -17 dBm at 622 MHz).

V. Conclusion

We have designed a broad-band PLL CDR for burst-mode applications. A time-domain model was used to design the CDR. The model was verified experimentally and a phase acquisition time of 100 bits was measured. This represents a greater than ten-fold improvement over corresponding SONET CDRs. Successful CDR was demonstrated and the tradeoff between lock acquisition time and PLL bandwidth resulted in the need for Manchester encoding. This work may be scaled to match the lock time and coding requirements of specific networks.

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