A Novel Bidirectional CMOS Transceiver for Chip-to-Chip Optical Interconnects

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***Abstract*—A novel bidirectional complementary metal–oxide–semiconductor (CMOS) transceiver for chip-to-chip optical interconnects operating at 2.5 Gb/s is proposed, which shares the common block of a receiver and a transmitter on a single chip. The share of the common block of two circuits makes it possible to save 55% or 20% of power dissipation, depending on the operating mode. The chip in 0.18-μm CMOS technology occupies an area of 0.82 $\times$ 0.82 mm^2, 70% of the total area of a typical unshared transceiver chip. The transmitting and receiving modes of operation show −3-dB bandwidths of 2.2 and 2.4 GHz and electrical isolations of −28 and −40 dB, respectively.**

***Index Terms*—Bidirectional, complementary metal–oxide–semiconductor (CMOS) integrated circuits, optical interconnections, transceivers.**

I. Introduction

THE EXPLOSIVE increase in signal processing speed will result in bandwidth limitations for metal-based interconnections on printed-circuit boards (PCBs) due to signal attenuation and distortion, electromagnetic interference, crosstalk, and power dissipation [1]. To solve these problems, optical interconnection on PCBs has been studied as a promising solution [2]–[5]. The interconnection architectures for chip-to-chip optical link on an optical PCB (OPCB), for example in our previous works [4], [5], consist of photodiodes (PDs) and front-end amplifiers in a receiver (Rx) module, vertical-cavity surface-emitting lasers (VCSELs), and driver ICs in a transmitter (Tx) module. To send and receive data via the optical link between large-scale integration (LSI) chips (e.g., CPU and memory), both multiplexed input and output signals in time division should be bidirectionally transmitted through one input–output (I/O) pin. However, the conventional works [6], [7] have employed separated unidirectional chips such as a pair of Tx and Rx ICs for parallel optical interconnection. In that case, the overall power dissipation and the occupied packaging area of parallel interconnection systems increase. To alleviate these problems, we have tried to integrate the Tx and Rx on a single chip by employing a selection switch (SW) and using a proposed common limiting stage. The proposed circuit integrated on a complementary metal–oxide–semiconductor (CMOS) chip is called a bidirectional-transceiver (Bi-TRx) in our letter. The Bi-TRx chip fabricated in 0.18-μm CMOS technology demonstrates the performance of an optical transceiver with bidirectionality by using the selection SW and provides lower power dissipation, more economical chip area, and a small packaging area by employing the proposed design strategy.

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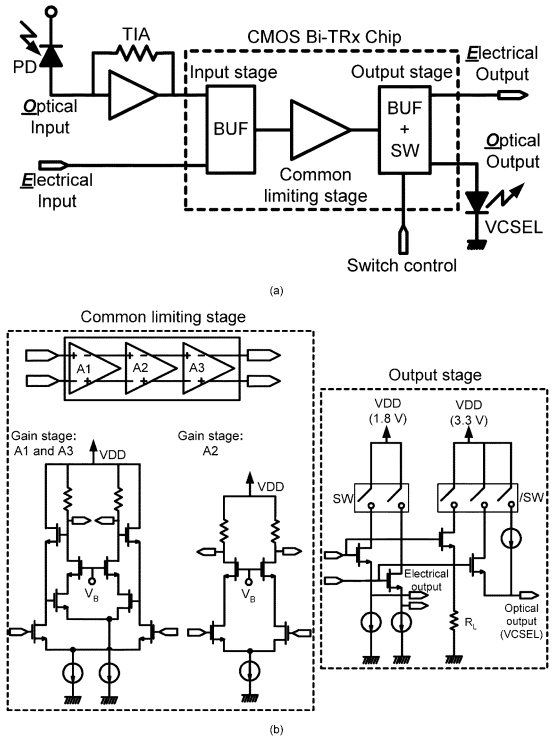

Fig. 1. (a) Proposed architectural configuration of bidirectional CMOS transceiver. (b) Detail circuit of common limiting stage and output stage.

II. Circuit Design

A typical limiting amplifier on the Rx part, for amplifying and reshaping the output signal of a transimpedance amplifier (TIA), consists of an input stage, a limiting amplifier stage, and an output stage. On the Tx part, the typical structure of the driver is similar to that of the limiting amplifier except that the output stage directly drives the VCSEL with sufficient bias and modulation current. Hence, we have tried to share the common block (limiting stage) between the limiting amplifier and the driver in this letter. It is a feasible design strategy since the optical input for the Rx mode and the electrical input for the Tx mode are multiplexed in time division for chip-to-chip optical link. As shown in Fig. 1(a), the proposed CMOS Bi-TRx architecture consists of input stages for an electrical signal and an optical

signal, a common limiting stage, and output stages with the selection SW. The Bi-TRx interfaces with external components, namely the PD and TIA on the Rx side, and the VCSEL on the Tx side.

The common limiting stage must be capable of sufficiently amplifying a small signal swing with adequate gain for the Rx mode and providing limited signal amplitude to drive the VCSEL for the Tx mode. In order to meet these requirements, the common limiting stage is designed to offer sufficient gain and bandwidth for the input signal, and the output stage is designed to interface the circuit with the subsequent input stage. The common limiting stage has three stages in this letter. In Fig. 1(b), both the first and third stage are adopted to achieve high gain and bandwidth using a Cherry–Hooper topology modified with an inner cascode amplifier. The inner cascode stage is a cascade of a common source amplifier and a common gate amplifier, which offers the high bandwidth by minimizing the Miller capacitance. For the second stage, a common source differential amplifier is used to provide higher gain.

Sharing this common limiting stage makes it possible to save as much power dissipation as it consumes in each operating mode and contribute to the chip-area reduction of over 30% compared to an unshared transceiver in the practical circuit simulation and layout design.

The output stage consists of the electrical buffer and the optical output driver as shown in Fig. 1(b). The electrical buffer is composed of a source follower and provides an impedance matching with subsequent circuit. The optical output driver consists of an open-source driver to modulate VCSEL current, a current source to deliver a prebias current to the VCSEL, and a source follower with resistive load $(R_L \approx 50\ \Omega)$ as a dummy driver as shown in Fig. 1(b). One of both outputs is selected by the SW depending on the operating mode. Especially in this letter, a careful design is required for isolation between the enabled and the disabled ports, since the disabled input may affect the output through the shared circuit block. The disabled signal, if any, feeding to the Bi-TRx circuit could be regarded as a noise, in which the effect could be minimized by using a differential pair in the circuit.

While the electrical output buffer uses a 1.8-V supply, the optical output driver operates at a supply voltage of 3.3 V to accommodate comparatively high forward voltage of the VCSEL.

III. Measurement Results

The Bi-TRx is fabricated in 0.18-μm CMOS technology and tested on-wafer using GGB microwave probes. Frequency response and eye-diagram measurements are performed using the Agilent 8703B lightwave component analyzer, Anritsu MP1763B pulse pattern generator (PPG), Agilent 86100A oscilloscope (OSC), and Tektronix SD-43 O/E converter for 850-nm wavelength, respectively.

Fig. 2 shows a whole chip photograph for the Bi-TRx. The occupied chip area is 0.82×0.82 mm^2. The design strategy that shares the common block of the limiting amplifier and the driver contributes to a chip-area reduction of over 30% and makes it possible to save 55% or 20% of power dissipation, depending on the Tx and Rx mode compared to the unshared transceiver.

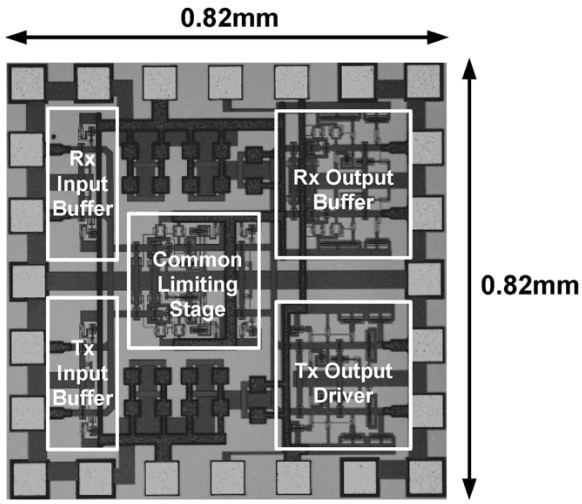

Fig. 2. Chip photograph of Bi-TRx.

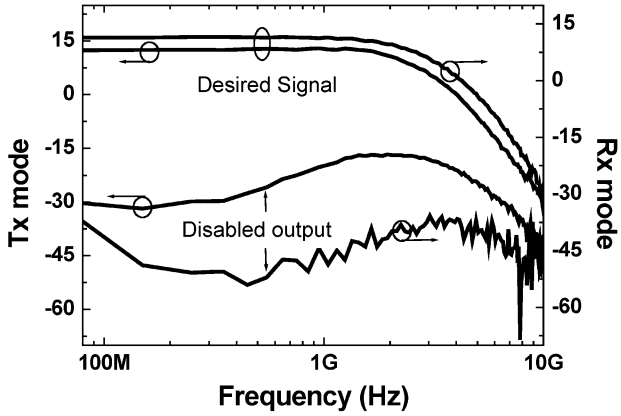

Fig. 3. Frequency response: Small-signal gain of the enabled output and isolation between the disabled output and the enabled output corresponding to Tx and Rx operating modes (y axes in decibels).

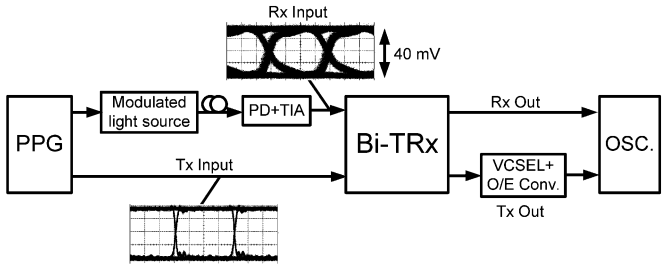

Fig. 4. Experimental setup.

Fig. 3 depicts the frequency response of two operating modes of the Bi-TRx chip. The -3-dB bandwidths of the Tx and Rx modes are 2.2 GHz and 2.4 GHz, respectively. From the small signal measurement, the disabled outputs for the Tx or Rx modes are isolated with -28 and -40 dB, respectively, from the enabled outputs.

The performance of the Bi-TRx is evaluated in the experimental setup shown in Fig. 4. The Bi-TRx chip is interfaced with the VCSEL on the Tx output side and the PD and the TIA on the Rx input side, respectively.

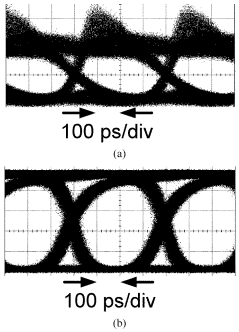

Fig. 5. Measured 2.5-Gb/s eye diagrams for the (a) Tx and (b) Rx operating modes (vertical: 100 mV/div).

Fig. 5(a) and (b) illustrates a measured optical nonfiltered eye diagram of the Bi-TRx coupled VCSEL for the Tx mode and a measured electrical output eye diagram of the Bi-TRx connected with the PD and the TIA for the Rx mode in a 2.5-Gb/s pseudorandom binary sequence input with pattern length of $2^{31}-1$, respectively. The measured results for the Tx and Rx modes are summarized as follows: horizontal eye openings of 0.79UI (317 ps) and 0.71UI (285 ps), peak-to-peak jitters of 83 and 115 ps, respectively, and a bit-error rate (BER) of less than 10^{-12} at 2.5 Gb/s.

IV. Conclusion

In this letter, a novel bidirectional transceiver for 2.5-Gb/s optical interconnects has been proposed and demonstrated in 0.18-μm CMOS technology. It provides both transmitting and receiving modes of operation on a single chip, showing -3-dB bandwidths of 2.2 and 2.4 GHz, and small-signal isolations of -28 and -40 dB between operating modes, respectively. The share of the common block between a limiting amplifier and a driver helps to save 55% or 20% of power dissipation depending on each operating mode. The chip occupies an area measuring 0.82×0.82 mm^2, 70% of the total area of an unshared transceiver chip.

References

[1] M. Forbes, J. Gourlay, and M. Desmulliez, "Optically interconnected electronic chips: A tutorial and review of the technology," *Electron. Commun. Eng. J.*, vol. 13, no. 5, pp. 221–232, Oct. 2001.

[2] I.-K. Cho, K. B. Yoon, S. H. Ahn, M. Y. Jeong, H.-K. Sung, B.-H. Lee, Y. U. Heo, and H.-H. Park, "Board-to-board optical interconnection system using optical slots," *IEEE Photon. Technol. Lett.*, vol. 16, no. 7, pp. 1754–1756, Jul. 2004.

[3] F. Mederer, R. Jager, H. J. Unold, R. Michalzik, K. J. Ebeling, S. Lehmacher, A. Neyer, and E. Griese, "3-Gb/s data transmission with GaAs VCSEL's over PCB integrated polymer waveguides," *IEEE Photon. Technol. Lett.*, vol. 13, no. 9, pp. 1032–1034, Sep. 2001.

[4] B. S. Rho, H. S. Cho, S. Kang, H.-H. Park, S.-W. Ha, and B.-H. Rhee, "PCB-compatible optical interconnection using 45°-ended connection rods and via-holed waveguides," *J. Lightw. Technol.*, vol. 22, no. 9, pp. 2128–2134, Sep. 2004.

[5] M. H. Cho, S. H. Hwang, H. S. Cho, and H.-H. Park, "High-coupling-efficiency optical interconnection using a 90°-bent fiber array connector in optical printed circuit boards," *IEEE Photon. Technol. Lett.*, vol. 17, no. 3, pp. 690–692, Mar. 2005.

[6] T. Nagahori, K. Miyoshi, Y. Aizawa, Y. Kusachi, Y. Nukada, N. Kami, and N. Suzuki, "An analog front-end chip set employing an electro-optical mixed design on SPICE for 5-Gb/s/ch parallel optical interconnection," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1984–1991, Dec. 2001.

[7] K. Kaminishl, H. Furuyama, K. Kojima, and K. Hirakawa, "Si bipolar 3.3 V transmitter/receiver IC chip set for 1 Gb/s 12-channel parallel optical interconnects," in *Dig. IEEE Int. Solid-State Circuits Conf.*, Feb. 1999, pp. 376–377.