System-Level Test and Yield Improvement for Optoelectronic-VLSI Chips

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***Abstract*—Some of the unique issues involved in testing transmitter and receiver circuits for optoelectronic-very-large-scale-integrated (OE-VLSI) applications are reviewed. In particular, the problem of testing OE-VLSI chips prior to optoelectronic device integration is outlined. Based on circuit-level approaches such as fault sensitization and novel system-level testing methodologies, the first OE-VLSI chip with testable transmitters, receivers and digital circuitry was designed in 0.35-μm CMOS. The operation of the ASIC was verified experimentally and a fault-coverage greater than 80% is obtained, for a test time in the hundreds of microseconds range. Yield improvements ranging from 10% to 25% are predicted.**

***Index Terms*—Design for testability, fault diagnosis, optoelectronic devices, optoelectronic-very-large-scale integration (OE-VLSI), yield estimation.**

I. Introduction

OPTOELECTRONIC-VLSI (OE-VLSI) involves the integration of OE devices (OEDs) on digital CMOS VLSI systems to complement or replace traditional electrical I/O. This additional fabrication step (usually heterogeneous integration, such as flip-chip bonding [1], [2]) is risky and decreases the yield of the ASIC, thus increasing costs dramatically. In order to make this technology commercially viable, conventional testing of the digital circuitry in isolation is not sufficient. It must also be possible to test large arrays of transmitter and receiver circuits prior to OED integration to eliminate the cost of performing heterogeneous integration on dead chips and increase the post-integration yield.

This paper first reviews testability and circuit-level test issues in OE-VLSI systems. This includes a discussion on a circuit-level test approach based on fault sensitization and detection with 1-bit analog-to-digital converters (ADCs). Secondly, a system-level scheme is proposed leading to the first implementation of an OE-VLSI ASIC with fully testable optical transceivers and digital circuitry. This chip was fully characterized experimentally and the results are presented. Finally, yield figures are extrapolated to validate the usefulness of the proposed testing approaches.

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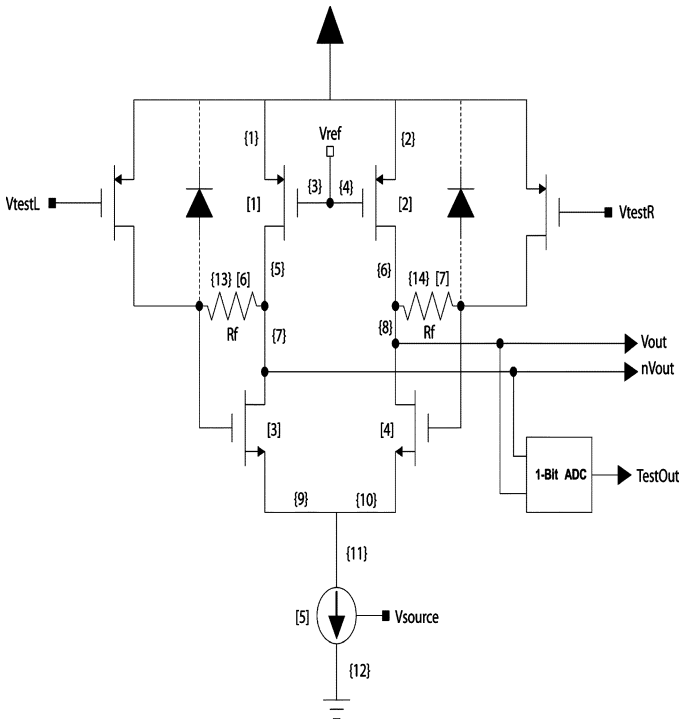

Fig. 1. Schematic of the transimpedance preamplifier, including comparator, test structures and faults.

II. Testability Issues and Circuit-Level Test

The testing of OE-VLSI chips is complicated by several issues unique to the technology. The OEDs are an integral part of the chip and their absence severely hinders testability. One proposed solution to this issue involves the addition of test structures in parallel with the intended location of the OEDs after heterogeneous integration, as shown in Fig. 1. These test structures essentially inject photocurrents in the receivers or provide a path for the drive currents in the transmitters. This approach was implemented in a 1080 channel OE-VLSI system demonstrator for both the optical transmitters and receivers [3]. Although this allowed for basic testability of the transceiver arrays, it was not sufficient to determine the type of faults present (open-circuit, bridging), and, more importantly, was incapable of pinpointing the fault location. Such precise diagnosis could be important for debugging designs and detecting fault-prone layouts.

In addition to the test structures mentioned earlier, additional test structures are required to increase the potential of detecting and determining the nature and location of faults in the transceiver arrays. Digital testing usually involves the injection of maximum fault coverage vectors into input/output flip-flops of combinational logic. Similarly, the transceiver test structures must be capable of detecting faults and generating binary output result vectors similar to conventional digital test outputs and compatible with existing test equipment. This can be achieved by adding one or more 1-bit ADCs to the optical receivers and transmitters. The two inputs of the ADC are connected to nodes in the circuits where differential signals are expected under fault-free operation. By varying the input levels of the circuit under test, the two voltage nodes under test vary and are compared and a digital one or zero is generated. As most faults will pull a node to the power rails, the differential nature of the signals is disrupted by a fault and its detection is possible. Signal differences as low as 50 mV could be detected with the 1-bit ADCs. Through careful placement of the comparator and analysis of the circuit under test, most of the open-circuit and bridging faults of a particular circuit topology can be detected. A more in-depth description of this methodology can be found in [4], [5].

An overview of the circuit-level testing approach just described is shown in Fig. 1 for a typical transimpedance preamplifier commonly used in optical receivers. Only differential topologies were considered as these are better suited for OE-VLSI systems [6]. The additional test structures were designed to consume no static power when the circuit is in normal operation. Only open-circuit ({ } in Fig. 1) and bridging faults ([ ] in Fig. 1) were considered [7], and are shown in Fig. 1. By varying VtestR, VtestL, Vref, and Vsource between high and low digital levels in various combinations, fault coverage from 80% to 90% could be achieved for a layout overhead between 35% and 65%, depending on the circuit topology. Layout overhead includes the addition of 1-bit ADCs, in-parallel OED replacement circuits and reference voltage generators for nondifferential circuit testing.

III. System-Level Test

The circuit-level testing approaches presented in the previous section were verified experimentally and their operation was validated. In order to evaluate this approach in a system-level context and to demonstrate its compatibility with conventional digital testing procedures, an OE-VLSI chip was designed and manufactured in a three metal, single poly CMOS 0.35-μm process. The chip is composed of fully testable optical transmitters and receivers serving as input/output (I/O) channels for a 64-bit inputs, 128-bit output arithmetic unit (AU) capable of performing addition, subtraction and multiplication on the two input vectors. A layout and architectural view of the chip is provided in Fig. 2.

Compatibility of the circuit-level testing methods with digital combinational logic was achieved through the use of serial scan chains (SSCs) as an interface between the AU and the transmitters and receivers [8]. The scan chains serve mostly as input/output registers to the AU and do not add any testing

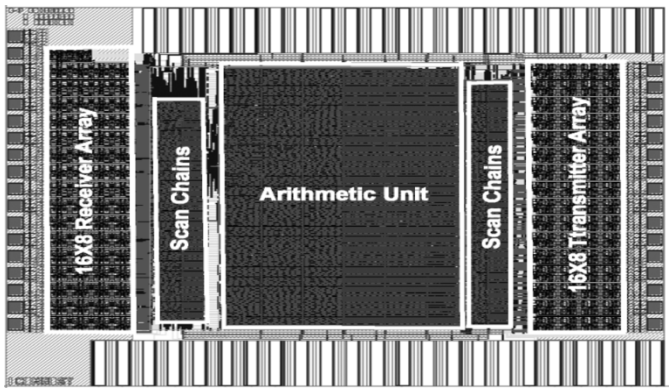

Fig. 2. Layout and architectural view of the OE-VLSI test chip.

layout overhead. The scan chains used for control bits add a small layout overhead which is already included in the number stated in Section II. All testing with the chip was conducted using the various scan chains. These SSC are highly flexible and can be used for multiple functions, including the scan in of control bits for the receiver and transmitters, scan in of test vectors and scan out of binary test results. The various functionalities of the chip are illustrated in Fig. 3. In addition, SSC provides the ability to trade-off test speed and electrical pad count, such that each design can be optimized for test speed, while maintaining a core-limited chip.

Other features of the chip include additional receivers for two optical clocks and for the operation-select bits of the arithmetic unit. The operator can choose between global and synchronous optical clocks or local electrical clocks. The same applies for the operation-select bits of the AU. The scan chains are expected to operate at a clock speed of at least 100 MHz. They vary in length between 32 and 184 bits.

A typical test cycle for this OE-VLSI system included the scan in of the transceiver control bits, the scan in of input test vectors, some time allocation for the stabilization of analog signals in the transceivers and the scan out of test results, and comparison with the expected results combined with pass or fail determination. Some test cycles might skip one of these steps. For example, testing the receiver array did not require any input test vector, as its input values are imbedded in the control vectors, while the testing of the AU did not need any control bits to be scanned in. Depending on the section of the chip under test, a test cycle varied between 216 and 312 clock cycles.

IV. Test Results and Yield Improvement

The test techniques implemented on the test chip were validated. Bare dies were wire bonded in pin-grid array (PGA) packages and electrical test was performed. Although passivation windows were included on the chip for the heterogeneous integration of the OEDs, this step was not performed. The fault-free status of several chips was verified for several test cycles and repeatable measurement results were obtained. As the OED integration was not completed, no statistical data on final OE-VLSI chips could be obtained.

On the other hand, experiments show that the proposed testing technique works. This necessarily leads to making theoretical yield improvement predictions resulting from the

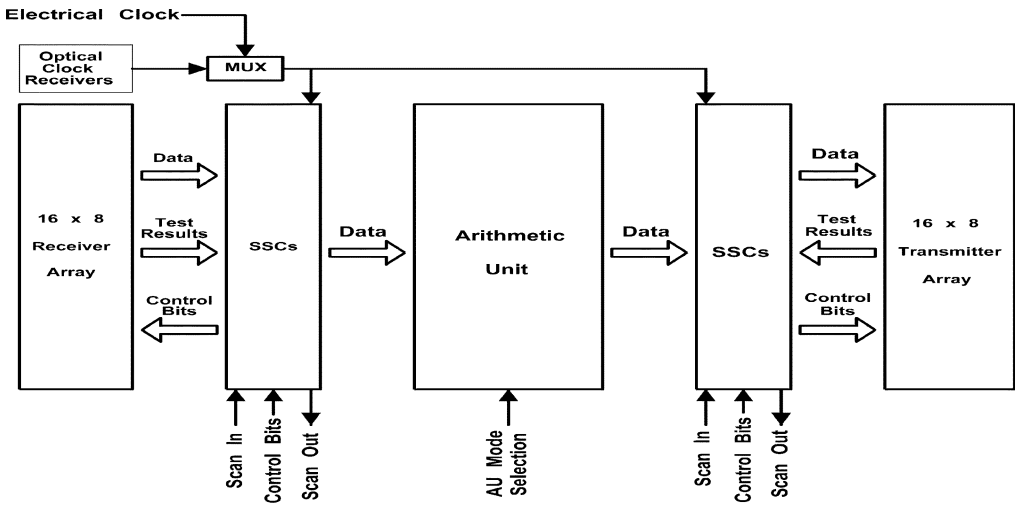

Fig. 3. Illustration of chip functionalities.

TABLE I
SUMMARY OF KEY TEST CHIP METRICS

	Value
Static power consumption under test	4.26 W
Static power consumption under normal operation	3.23 W
Fault coverage	81.3 %
Effective fault coverage	66.9 %
Estimated test time	160 μs
Test Chip Area	11.82 mm^2
Total test structure layout overhead	6.5 %

proposed test methodology. Similarly, it was not possible to evaluate the maximum data rate achievable by the system. On the other hand, simulations suggest that a data rate penalty close to 20% should arise from the addition of multiple 1-bit ADCs in the transceivers data path. The benefits of increased yield on a large number of parallel channels outweigh the slight decrease in data rate of individual channels.

Several key parameters and metrics pertaining to the test chip are summarized in Table I. An overall test time of approximately 160 μs is estimated for the chip assuming a 100 MHz clock rate. This includes the verification of the functionality of the scan chains, the testing of the AU with four input combinations for each operation, and the full testing of the receiver and transmitter arrays, including bias and feedback circuitry. The fault coverage represents the percentage of the faults considered that could be sensitized successfully. The effective fault coverage considers faults in the test structures, leading to throwing good dies with faulty test circuits. This results in a slight reduction of the fault coverage. ADCs and voltage reference generators were shut down in normal operation, resulting in a significant decrease of power consumption. Due to the modularity of the design, all metrics should scale linearly with increased array size/width of data path.

The usefulness of this testing approach resides in the improvement in post-OED integration yield that can be achieved. This result is illustrated in Fig. 4, where a typical pre-OED integration yield curve based on a simple negative binomial model is shown (solid curve) [9]. Although not optimized for the technology used in this design, this model is sufficient to illustrate the yield improvements that can be achieved using the proposed testing methodology. On the figure, the number of logic devices is equivalent to the number of transistors in a channel, including the transmitter, receiver and digital section. Assuming a yield of 96% for the OEDs [3], the post-OED integration yield per channel without testing is shown (dotted curve). When testing is implemented, most of the faulty CMOS chips are rejected prior to OED integration, resulting in a significant increase in overall post-OED integration yield (dashed curve). This curve was obtained using (1) below, where FY is the post-OED integration yield with testing, OY is the OED yield, IY is the initial CMOS yield, and FC is the test fault coverage

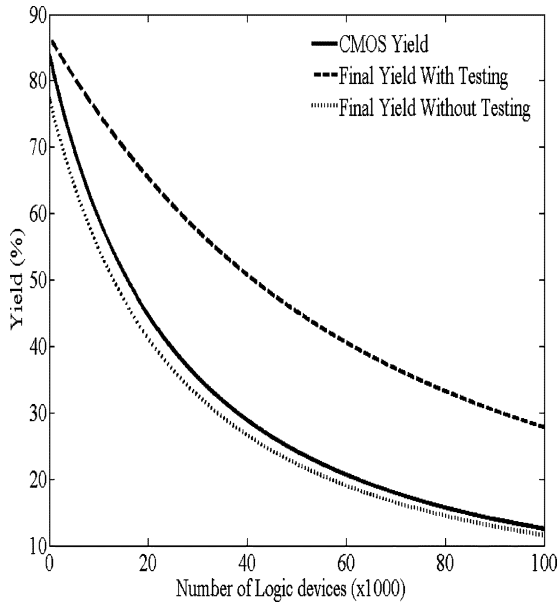

Fig. 4. Predicted post-OED integration yield improvement using the proposed test methodologies.

$$\mathrm{FY} = \mathrm{OY}^2 * \frac{\mathrm{IY}}{1 - (\mathrm{EFC} * [1 - \mathrm{IY}])}. \quad (1)$$

V. Conclusion

We have described the first implementation of a fully testable OE-VLSI ASIC. This system includes testable receiver and transmitter arrays as well as SSCs for conventional digital testing compatibility. The operation of the test chip was verified experimentally and test cycle times as low as 160 μs are estimated. Moreover, the proposed testing approach could improve the post-OED integration yield of OE-VLSI systems significantly.

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