Multiuser OCDMA System Demonstrator With Full CDR Using a Novel OCDMA Receiver

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***Abstract*—We report the first multiuser optical code-division multiple-access (OCDMA) system demonstrator with full clock and data recovery using a novel OCDMA receiver. We achieve receiver sensitivities of −19.1, −16.3, and −9.2 dBm for one, two, and three users, respectively, at a BER $\leq 10^{-10}$ using a $2^{20}-1$ pseudorandom binary sequence. Our results show the viability of OCDMA as a transport technology for access networks.**

***Index Terms*—Clock and data recovery (CDR), optical code-division multiple-access (OCDMA), optical fiber communications, optical networks, optical receiver.**

I. Introduction

OPTICAL code-division multiple-access (OCDMA) is a promising technology for use in optical access networks carrying bursty and asynchronous traffic [1]. Two-dimensional (2-D) wavelength-time $(\lambda - t)$ OCDMA has been explored as a means to provide greater flexibility in code design, increase the number of simultaneous users, increase data throughput, and provide better scalability to accommodate more users [2]–[4]. To date, most or all OCDMA technology demonstrators have relied on the availability of a global clock in system implementation and testing, especially for performing bit-error-rate (BER) measurements [5]–[7], which is not representative of a real functional access network. For OCDMA to be a competitive alternative to conventional multiple-access schemes, such as time-division multiple-access (TDMA) and wavelength-division multiple-access (WDMA), full clock and data recovery (CDR) at the receiver end must be demonstrated. In this letter, we report the first multiuser OCDMA system demonstrator with full CDR. This is enabled by a novel OCDMA receiver that was designed using commercially available components. In addition to recovering the clock from the OCDMA signal, the receiver converts the multilevel return-to-zero (RZ) signal with a $1/N$ duty cycle (N is the number of time chips) to a binary nonreturn-to-zero (NRZ) signal for further processing. The OCDMA receiver allows digital logic circuits to process OCDMA data in the same way as if TDMA or WDMA had been used in the transport network.

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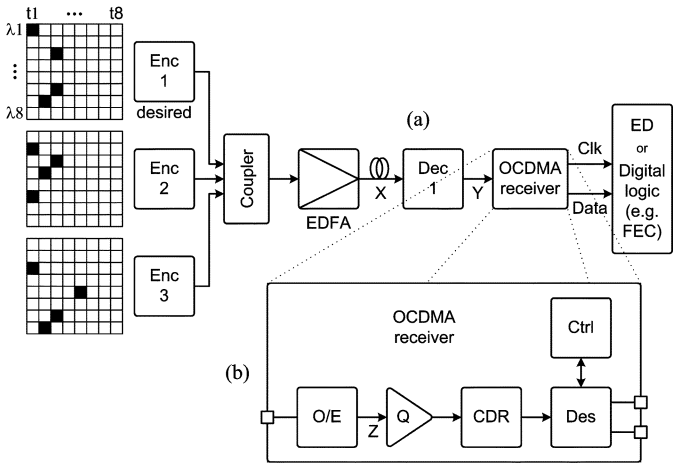

Fig. 1. (a) OCDMA demonstrator with CDR, (b) OCDMA receiver. ED: Error detector.

II. OCDMA System Demonstrator

A. Experimental Setup

Fig. 1(a) shows the OCDMA system that was implemented and tested. Unlike other OCDMA systems [5]–[7], no global clock is used at the receiving end to perform BER measurements. Instead, the clock is recovered from the data by the OCDMA receiver described in Section II-B.

The OCDMA system is based on the 2-D $\lambda - t$ depth first search codes (DFSCs) described in [4]. While many different 2-D $\lambda - t$ code families exist, we have focused on DFSCs since they possess the following key advantages: 1) the codes can be designed using fewer time chips and, thus, are able to support higher data rates and 2) since for a given code dimension a greater number of codes can be generated, they can fully exploit the gain provided by forward error correction (FEC) to allow for a large number of simultaneous users operating with good BER performance [4].

In our system demonstrator, we use codes having eight wavelengths, eight time chips, and a weight of four. The chip rate is OC-24 (1.244 16 Gb/s) and the bit rate is OC-3 (155.52 Mb/s). Of the 31 possible codes generated by the DFS algorithm, we use the three codes illustrated in Fig. 1(a). The two interferers (Enc 2 and 3) were chosen such that each has two wavelengths in common with the desired user (Enc 1), thereby making the task of identifying the autocorrelation peak more difficult (this represents a worst-case scenario among the 31 codes generated by the DFS algorithm). A "1" data bit is represented by a broadband pulse (modulated amplified spontaneous emisson from a

TABLE I
OCDMA SYSTEM DEMONSTRATOR PARAMETERS

Parameter	Value
Wavelength range	1547.6 nm - 1553.2 nm
Channel spacing	100 GHz (0.8 nm)
Data rate	155.52 Mbps (OC-3)
Chip rate	1.24416 Gbps (OC-24)
PRBS	2^{20}-1
Photoreceiver bandwidth	800 MHz

broad-band source) having a duration equal to the chip time; no power is transmitted for a "0" bit. The data from the different users are then optically encoded. The encoders and decoder are constructed using commercially available wavelength demultiplexers/multiplexers, power splitters, and combiners; the time delays are obtained by splicing appropriate lengths of fiber, each carefully measured to have less than $\pm 5\%$ of a time chip of error in order to minimize the effects of encoder/decoder mismatch [8]. The decoder (Dec 1) performs matched filtering before detection. Erbium-doped fiber amplifiers are used to amplify the signals. The target BER is 10^{-10} using a pseudorandom binary sequence (PRBS) length of $2^{20}-1$ for each user. All three users transmit at the same power. Various lengths of decorrelating fiber, corresponding to time shifts of 8 to 16 bits, are used to emulate different bit streams for each user. The system parameters are summarized in Table I.

B. OCDMA Receiver

The OCDMA receiver is made of five building blocks [see Fig. 1(b)]: a photoreceiver (photodetector + transimpedance amplifier), a quantizer (Q), a SONET CDR, a $1:16$ deserializer (Des), and a controller (Ctrl). The quantizer and the CDR are from Analog Devices (part #ADN2819), while the deserializer is from Maxim-IC (part #MAX3885).

The quantizer applies a threshold on the incoming data in order to filter out multiaccess interference (MAI) from the interferers. The CDR recovers the clock at twice the chip rate, or OC-48, to accommodate the $1:16$ deserializer ($2.488\,32$ Gb/s$/16 = 155.52$ Mb/s). Clock recovery at OC-24 would also work, provided a $1:8$ deserializer is available. With equal rise and fall times, a $1:8$ deserializer is preferable since the autocorrelation peaks of the OCDMA signal are sampled in the middle. With unequal rise and fall times, it may be advantageous to sample the autocorrelation peaks at a slight offset from the middle. The $1:16$ deserializer allows this, at the cost of a higher bandwidth CDR (OC-48 instead of OC-24).

The $1:16$ deserializer produces a 155-MHz clock by dividing the clock output of the CDR by 16. It also converts the RZ signal with 1/8 duty cycle to an OC-3 NRZ signal. Port 1 of the 16-bit deserializer output serves as the OCDMA receiver output. Without the controller, data could appear on any one of the 15 unused ports of the deserializer output. When the link is first established, the controller configures the deserializer such that data is steered to Port 1. This is accomplished by monitoring activity on Port 1 and sending appropriate retiming/reframing signals to the synchronization input of the deserializer.

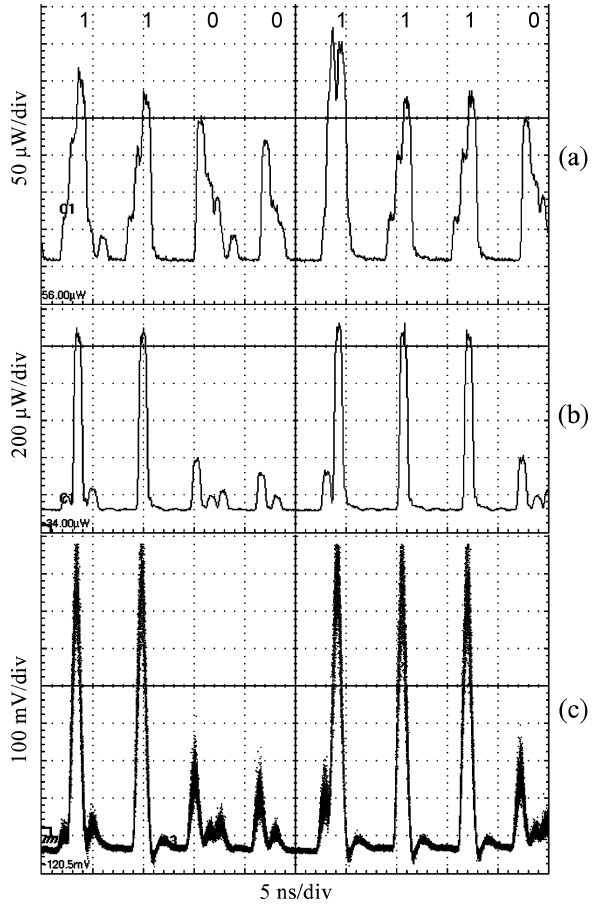

Fig. 2. (a) Three OCDMA encoded signals ("X" in Fig. 1) merged on the same fiber (8 bits of the $2^{20}-1$ PRBS are shown). (b) Decoded signal ("Y" in Fig. 1). (c) Photoreceiver output ("Z" in Fig. 1), just before the quantizer.

The OCDMA receiver can be used in OCDMA systems other that the one described here. The receiver supports chip rates of OC-3, OC-12, OC-48, Gigabit Ethernet (GbE), and 15/14 FEC rates. The supported bit rates depend on the number of time chips N in the OCDMA code and the availability of a $1:N$ deserializer. With higher speed electronics, the design can be scaled up to higher chip and/or bit rates. For example, a receiver built from a 10-Gb/s CDR and a $1:8$ deserializer could support a bit rate of 1.25 Gb/s (assuming eight time chips). Such a receiver could enable the use of OCDMA in gigabit passive optical networks (ITU-T G.984 GPON and IEEE 802.3ah EPON), which currently use TDMA as an access method. Considering that 1) multiaccess networks typically operate at slower data rates than long-haul networks, and 2) the design is based on off-the-shelf SONET components, this solution will leverage the development of 10- and 40-Gb/s electronics to support 1.25–5-Gb/s bit rates cost and time effectively.

III. MEASUREMENT RESULTS

Fig. 2(a) and (b) shows all three encoded and the decoded optical signals, respectively (measured with an optical sampling module having a 12.5-GHz bandwidth and $32\times$ averaging); Fig. 2(b) confirms that the reconstructed desired signal (autocorrelation peak) is indeed distinguishable from the MAI. The

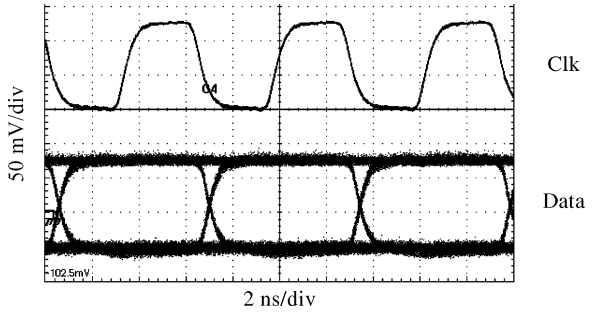

Fig. 3. Recovered clock and data. The width of the eye is about 6.4 ns, corresponding to a bit rate of 155.52 Mb/s (OC-3).

TABLE II
RECEIVER SENSITIVITY RESULTS

Case	Sensitivity[a] (dBm)	Power penalty (dB)
Desired user	-19.1	
Desired user + 1 interferer	-16.3	2.8
Desired user + 2 interferers	-9.2	9.9

[a]BER $\leq 10^{-10}$, 2^{20}-1 PRBS.

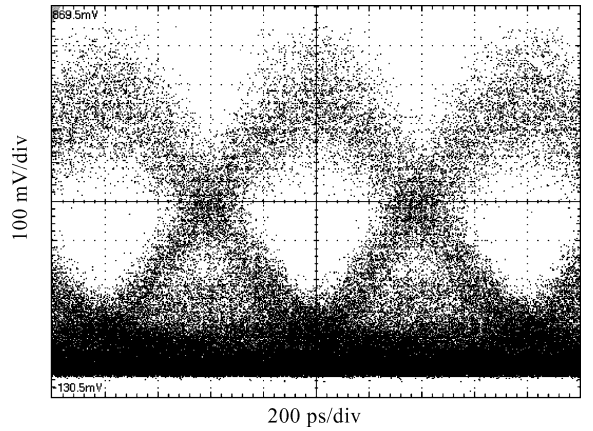

Fig. 4. Photoreceiver output ("Z" in Fig. 1) at receiver sensitivity (-9.2 dBm) with all three users present on the network. The width of the eye is about 800 ps, corresponding to a chip rate of 1.244 16 Gb/s (OC-24).

cross-correlation pulses in the decoded waveform correspond to the interfering wavelengths that are retained by the decoder.

Fig. 2(c) (no averaging, 10-s persistence) shows the signal after the photoreceiver, which has a bandwidth of 800 MHz. The output of the OCDMA receiver, after 3R regeneration, is shown in Fig. 3. The measured root-mean-square (rms) jitter on the recovered clock was 15.6 ps (0.002 UI rms). The receiver not only recovers the clock from the OCDMA signal, it also converts the multilevel RZ signal with a duty cycle of 1/8 to an OC-3 NRZ signal.

The sensitivity of the OCDMA receiver was measured using three different test conditions, which are listed in Table II. Fig. 4 shows the eye diagram of the signal after optical-to-electrical (O/E) conversion (signal "Z" in Fig. 1) for the worst case scenario (desired user + two interferers). Note that the sampling oscilloscope was triggered at the chip rate in Fig. 4, whereas, it was triggered using the pattern sync signal from the pulse pattern generator in Fig. 2(c). For the situation with the desired user only, the measured sensitivity was -19.1 dBm at a BER $\leq 10^{-10}$ using a PRBS of length $2^{20} - 1$. The introduction of one and two interferers caused power penalties of 2.8 and 9.9 dB, respectively. We attribute the power penalties largely to MAI and beat noise. MAI is expected to vary with the OCDMA codes being used, while beat noise is known to limit performance in OCDMA networks [9]. We obtained a sensitivity of -15.5 dBm when only the desired user was transmitting over 7 km of single-mode fiber (with no dispersion compensation), corresponding to a power penalty of 3.6 dB relative to the back-to-back case.

IV. CONCLUSION

We have described a multiuser OCDMA system demonstrator with full CDR using a novel OCDMA receiver. No global clock was used in the system. The receiver functionality was demonstrated in a 2-D $\lambda - t$ OCDMA system, but can be used in other OCDMA systems. The receiver uses commercially available components and allows OCDMA to be compatible with digital logic circuits developed for TDMA and WDMA networks. Our results show the viability of OCDMA as a transport technology for access networks.

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REFERENCES

[1] A. Stok and E. H. Sargent, "Lighting the local area: Optical code-division multiple-access and quality of service provisioning," *IEEE Network*, vol. 14, no. 6, pp. 42–46, Nov./Dec. 2000.

[2] L. Tančevski and I. Andonovic, "Wavelength hopping/time spreading code division multiple access systems," *Electron. Lett.*, vol. 30, no. 17, pp. 1388–1390, 1994.

[3] A. J. Mendez, R. M. Gagliardi, V. J. Hernandez, C. V. Bennett, and W. J. Lennon, "High-performance optical CDMA system based on 2-D optical orthogonal codes," *J. Lightw. Technol.*, vol. 22, no. 11, pp. 2409–2419, Nov. 2004.

[4] R. M. H. Yim, L. R. Chen, and J. Bajcsy, "Design and performance of 2-D codes for wavelength-time optical CDMA," *IEEE Photon. Technol. Lett.*, vol. 14, no. 5, pp. 714–716, May 2002.

[5] R. P. Scott, W. Cong, K. Li, V. J. Hernandez, B. H. Kohlner, J. P. Heritage, and S. J. B. Yoo, "Demonstration of an error-free 4 × 10 Gb.s multiuser SPECTS O-CDMA network testbed," *IEEE Photon. Technol. Lett.*, vol. 16, no. 9, pp. 2189–2191, Sep. 2004.

[6] V. J. Hernandez, A. J. Mendez, C. V. Bennett, and W. J. Lennon, "Bit-error-rate performance of a gigabit Ethernet O-CDMA technology demonstrator (TD)," in *Proc. LEOS Annual Meeting*, Rio Grande, PR, 2004, Paper WE5.

[7] V. Baby, C.-S. Bres, L. Xu, I. Glesk, and P. R. Prucnal, "Demonstration of a differentiated service provisioning with 4-node 253 Gchip/s fast frequency-hopping time-spreading OCDMA," *Electron. Lett.*, vol. 40, pp. 755–756, 2004.

[8] R. Adams, "Analysis and implementation of a two dimensional wavelength-time optical code-division multiple-access system," M.Eng. thesis, McGill Univ., Montreal, Canada, 2004.

[9] X. Wang and K. Kitayama, "Analysis of beat noise in coherent and incoherent time-spreading OCDMA," *J. Lightw. Technol.*, vol. 22, no. 10, pp. 2226–2235, Oct. 2004.