

Experimental techniques using optically enabled ring oscillators

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We present a method for characterizing transceiver performance in parallel optical data links. By establishing a bidirectional link between two optically enabled chips, the conditions for a ring oscillator are made possible. We propose this technique as a means of measuring the sensitivity of transceiver latency to controlled variables such as temperature, optical output power, supply voltage, and device misalignment. This method is noninvasive and independent of the packaging, circuit topology, and optical medium used. The technique is demonstrated experimentally, and results are compared with a simulation. © 2004 Optical Society of America

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1. Introduction

Improved integration of optical transmitters and receivers with traditional chip fabrication techniques has produced new technologies for interchip optical communication. These technologies are aimed at circumventing both the growing limitations of electrical interconnects and the increasingly restrictive pin counts of ever-shrinking, more-sophisticated chips. Research efforts have yielded chips that are fitted with upwards of one thousand optical receivers and surface-normal transmitters [such as the vertical-cavity surface-emitting laser (VCSEL)] making use of the third spatial dimension for communication. Such arrays demonstrate the potential for high data rates with minimal crosstalk.

In the operation of a parallel optical data link, it is desirable that the elements of the array behave synchronously. Skew arising between array elements will reduce the likelihood that all bits are ready to proceed at each clock edge. Poor synchronicity of data in a parallel link limits the ability to operate the link at high data rates. Thus the capability to mea-

sure latency (and, by implication, skew) in a parallel optical data link is of significant value in testing new and existing transceiver designs. However, it is prohibitively difficult, owing to capacitive loading effects and the inherent speed limitations of complementary metal-oxide semiconductors (CMOS) devices, to make such precise latency measurements by conventional electronic means.

Several approaches to this problem have been investigated.^{1,2} One such approach makes use of an electrical ring oscillator.¹ Traditionally, such oscillators have been used to obtain information about the latency of a given transistor technology. Such an oscillator operates on the principle that an odd number of inverters in a closed-loop signal path results in steady-state sinusoidal oscillation at the maximum possible frequency. The oscillation period is the sum of all electrical delays in the loop, including those of the inverters. We extended this idea to make use of the optical domain. By allowing an inverter in the ring to also serve as a transmitter for a multiple quantum-well (MQW) modulator, this technique uses optical readout to make noninvasive measurements of the oscillation period. We successfully used this technique to measure inverter propagation delay and investigate load capacitance effects. The principle is illustrated in Fig. 1(a).

In another approach,² precise latency measurements with picosecond resolution were achieved by use of short optical pulses (return-to-zero signaling format). To obtain these measurements, a pump-probe setup was assembled in which a mode-locked laser was incident upon an on-chip detector. The subsequent voltage pulse train generated by the re-

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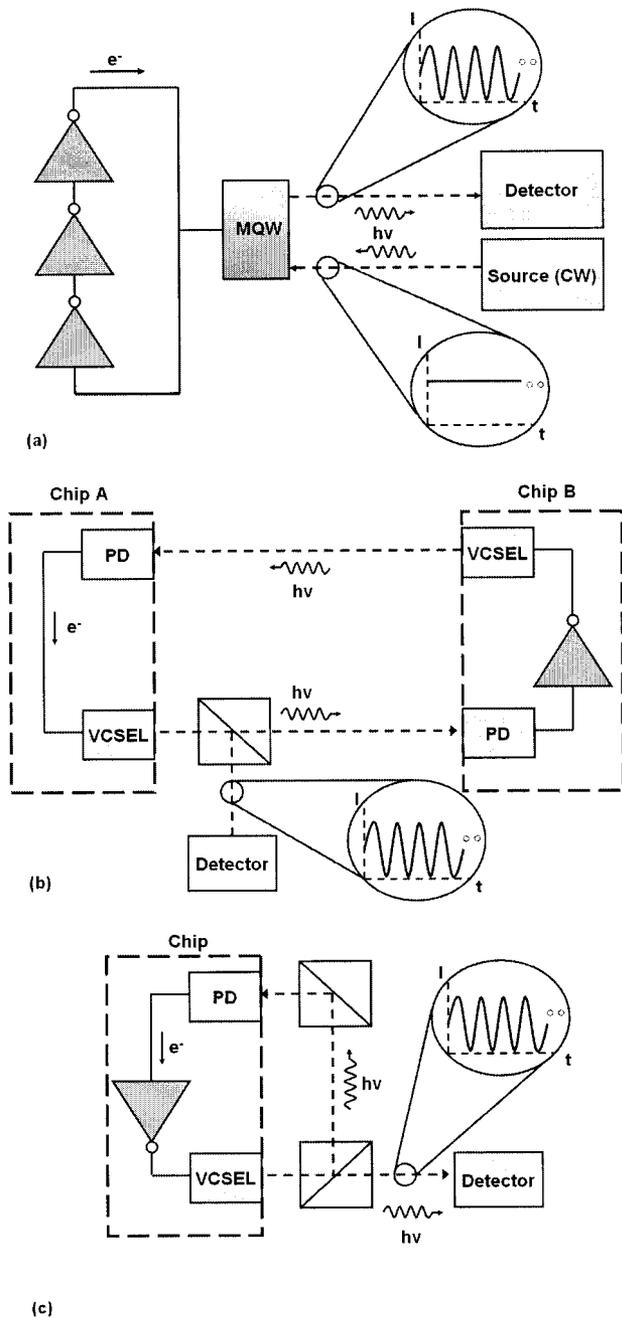


Fig. 1. Illustration of possible ring oscillator setups. (a) Electrical ring oscillator with optical readout. A cw laser beam is encoded with the oscillation by an MQW reflector and then detected for measurement. (b) OERO (two chips) using on-chip sources and detectors. (c) OERO using one chip only.

ceiver was used to modulate an MQW reflector. By probing the reflector with a delayed copy of the input beam, precise latency measurements were possible. In this and other works, return-to-zero signaling is shown to yield certain performance improvements over non-return-to-zero signaling.^{3,4}

We extend the principle of noninvasive measurement using a ring oscillator to include the full optical-to-electrical-to-optical (O-E-O) signal path, including on-chip detectors and conventional, laser-

based transmitters instead of MQW inverters, in order to achieve a generic, system-level means of characterizing transceiver performance. Although the technique presented is theoretically independent of the signaling format, the current state of fully integrated source technology precludes the use of short optical pulses, and as a result this technique is presently limited to non-return-to-zero signaling.

Our approach demonstrates the concept of an optically enabled ring oscillator (OERO). The remainder of this paper introduces the general operational principles of an OERO and provides the details of one specific OERO implementation as applied in an experimental context, including a comparison between simulated and experimental data. This paper is organized as follows. Section 2 describes the general principles of an OERO system as well as the assembly and packaging requirements of one such system. Section 3 discusses the optical system used for imaging and details the alignment procedure of the OERO. Section 4 contains a discussion of the experimental results obtained and a comparison to simulation, as well as a discussion of measurement uncertainty and jitter. Section 5 concludes the paper.

2. OERO Principles and Assembly

By facing two optically enabled chips, a bidirectional link can be established, as shown in Fig. 1(b). With an odd number of inverters in the signal path and the proper biasing, the system will achieve steady-state oscillation. The period of oscillation is the sum of all delays in the ring as follows:

$$T_{\text{OSC}} = 2(L_{\text{RX}} + L_{\text{TX}} + L_{\text{INV}} + L_{\text{EI}} + \text{TOF}), \quad (1)$$

where L_{RX} , L_{TX} , L_{INV} , and L_{EI} represent the delays of the receiver, the transmitter, the inverter, and the electrical interconnects, respectively, and TOF is the optical time of flight. The contribution of the optical TOF to the oscillation period is significant and is a function of chip separation; flight delay can contribute roughly a nanosecond for a 40-cm chip separation, including travel time through optical elements in the system (a large chip separation exists to accommodate the imaging system, which will be discussed). However, the TOF is a fixed delay that is independent of optical power levels and temperature, among other factors. Thus, although this setup does not approach the picosecond resolution of previous work² (as shall be shown), it is nonetheless suitable for measuring changes in transceiver latency as a result of changes in externally controllable variables. Apart from characterizing transceivers, an OERO may be also applied to measure the latency of any digital circuit interposed between an existing optical input and output. It is also possible to create an OERO in the use of a single chip, as illustrated in Fig. 1(c).⁵ Such a system would exhibit a smaller TOF and could be implemented in free space (as depicted) or with use of a fiber waveguide.

The strength of this technique is its versatility,

because it is independent of transceiver circuit topology, device packaging, and optical transmission medium (free space or guided) and is applicable for both optically single-ended and differential systems. One limitation of the OERO is that because the oscillation period tends to be large (owing to the addition of fixed delays such as TOF), this technique would not be suitable for accurately measuring such high-speed electrical parameters as rise time.

To provide a demonstration of the assembly of an OERO, we discuss one possible implementation of this technique in an experimental context. The experiment consists of measuring changes in receiver latency with respect to changing incident optical power levels.⁶ This experiment is well suited for an OERO, because it is concerned with a relative measurement instead of an absolute measurement and it features an easily controlled variable (optical power throughput). A test chip was fabricated using 0.5- μm Ultra Thin Silicon (UTSI) CMOS process technology from Peregrine Semiconductor (San Diego, California), which employs an electrically insulating sapphire substrate. The chip contains four different receiver designs (one implementation in each chip corner) in order to investigate how changing optical input power level affects receiver latency. Each receiver circuit drives a small block of transistor logic that is externally controlled in software to act as either a buffer or an inverter. This is necessary because the operation of an OERO requires an odd number of inversions in the signal path; thus one chip in the setup acts to invert the signal, whereas the other chip simply buffers it. This buffer-inverter drives a transmitter circuit (all corners of the chip use identical transmitters in this experiment). The transmitters were externally controlled with use of switches for toggling VCSEL bias and modulation currents.

The chips were manually packaged in 100-pin pin-grid arrays (PGAs) along with 1×4 bars of VCSELs and photodetectors (PDs) abutted against the chip sides in the corner being tested. This abutment was possible because of the nonconductive nature of the chip substrate. Wirebond connections were added manually to connect the chip to the PGA and to the VCSEL and PD bars. A photograph of one packaged chip corner is shown in Fig. 2. The chip was designed for an optically differential signal. Only two of the optical elements on each bar were used, comprising one optically differential channel to and from each chip.

Two test chips in PGAs were inserted into test boards and mounted onto micropositioning stages with control over six axes of motion (three translational, three rotational). Because the optical system used for imaging was inverting (as will be discussed in Section 3), one board was rotated by 90° with respect to the other in order to properly image the VCSELs of one chip onto the PDs of the other and vice versa, as illustrated by Fig. 3. This inversion is of no further consequence to the establishment of optical

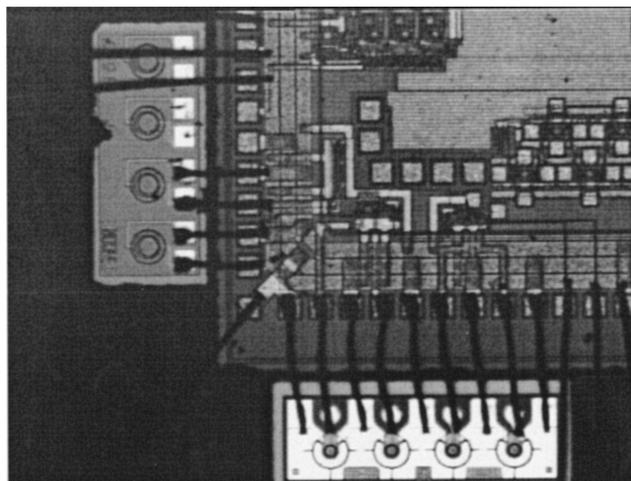


Fig. 2. Photograph of a packaged test chip corner with a 1×4 bar of VCSELs (bottom) and another of PDs (left).

channels, because two optical inversions occur during a single round trip.

3. Optical System

This section is concerned with the imaging and alignment requirements of a free-space OERO. An OERO does not, in principle, have to be free space and could be created with the use of fiber as the transmission medium. An in-fiber OERO removes the need for a bulky imaging system and would ease the complexity of alignment. Nevertheless, such a system would have its own challenges to overcome. It may be more difficult, for example, to characterize arrays of varying sizes by use of fiber than it would be to implement several simultaneous free-space OEROs between two chips.

The principle requirements of the optical system in a free-space OERO include: i) providing 1:1 imaging with minimized distortion over a sufficiently large

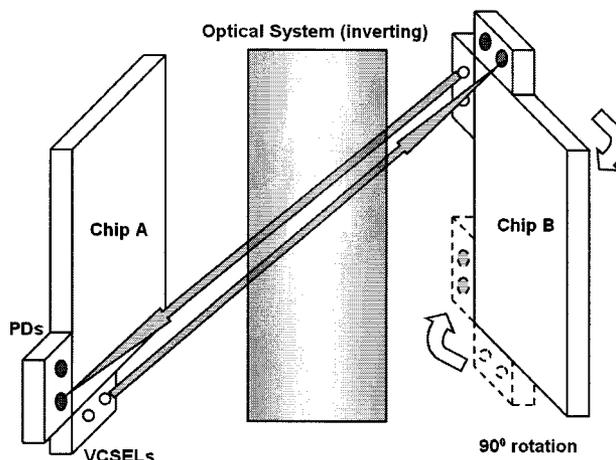


Fig. 3. Illustration of face-to-face identically packaged test chips. The rotation illustrated from starting position (dotted) is necessary to properly align the image of one chip with the inverted image of the other.

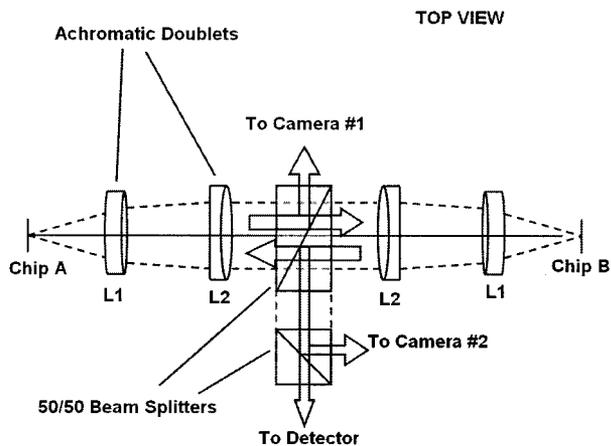


Fig. 4. Top view of OERO optical system. Cameras #1 and #2 image chips A and B, respectively.

object area to contain the lasers and detectors, ii) preserving bidirectional symmetry, and iii) facilitating the observation of both chips for visual alignment. The last requirement implies that achromatic lenses are preferable, since the VCSEL wavelength of 850 nm should remain spatially consistent with the visible-light image of the chip. The optical system used in the experiment consisted of a $4f$ telecentric, double-Petzval configuration, depicted in Fig. 4. This is an inverting system intended for 1:1 imaging. The details of the optical system are summarized in Table 1. This system was initially designed for a different imaging problem to accommodate rays that are as far off axis as 3.2 mm (representing a square object area of $4.5 \text{ mm} \times 4.5 \text{ mm}$) with a spot size of no greater than $20 \text{ }\mu\text{m}$.⁷ Since the object area of the experiment containing the VCSEL and PD bars is approximately $2 \text{ mm} \times 2 \text{ mm}$, this system is more than adequate for implementation in this OERO.

In the gap between the L2 lenses, where the light is approximately collimated, a beam splitter was inserted for imaging and detection. With the setup as in Fig. 4, it was possible to simultaneously observe both chips with use of CCD cameras, which aided in the alignment procedure. Each camera was preceded by a small focusing lens ($f = 40 \text{ mm}$). A photograph of the complete OERO system is shown in Fig. 5, including the detector used to spatially filter one optical channel for frequency measurement.

The first step in the manual alignment of an OERO is to locate the central optical axis. This is made

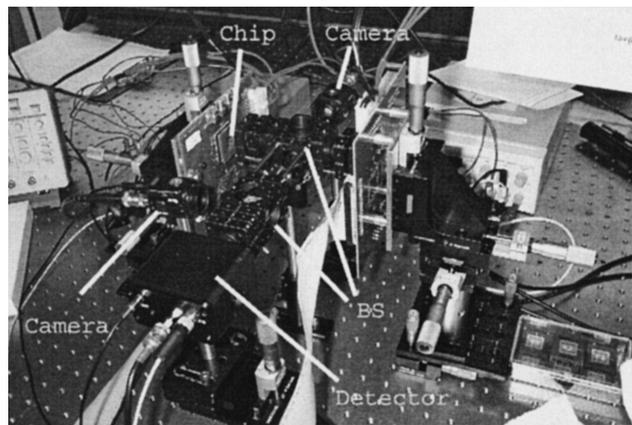


Fig. 5. Photograph of the assembled OERO. Two CCD imaging cameras and a photodetector are used simultaneously by using two beam-splitters (BS).

simpler by inserting an iris in the optical system and then observing each chip (using the CCD cameras) while the translational micropositioners are adjusted. The use of an iris also has the added benefit of reducing off-axis reflections. Once this coarse alignment has been established, the VCSELs of one chip are turned on, and the resulting spots on the opposite chip can be used to gauge how far off the alignment is. The quality and size of the spots created can be used to judge proper z distance of the chips from the optical system lenses. The angular micropositioner controls are adjusted (along with some compensation from the translational positioners) to yield a small, circular spot image on each chip located on the appropriate photodetectors. Once this has been established, it is possible to test the integrity of the optical link by toggling the VCSEL modulation current on a given chip. If the VCSELs are properly imaged onto the opposite chip's pair of photodetectors and sufficient optical power is delivered, the VCSELs of the targeted chip should also toggle. Fine tuning the alignment, once it has been established that both chips are working, is straightforward. A bidirectional link will spontaneously begin to oscillate (if an inversion has been set in the signal path) and both VCSELs on each chip will appear to be "on."

The spatial location and angle of the VCSEL and PD bars, as packaged on chip, are critical, and the two chips must be as similar as possible, because small angular deflections on chip are exaggerated to

Table 1. Optical System Properties

Lens	Model	Focal Length (mm)	Diameter (mm)	Thickness (mm)
L1	Edmund Scientific E32723	60.00	25.00	11.40
L2	Melles-Griot 01LAO114	80.011	31.0	9.50
	Obj/image-L1 (mm)	L1-L2 (mm)	L2-L2 (mm)	Chip-to-Chip (mm)
Distance	19.4	25.0	37.0	~170
Tolerance	N/A	0.1 in z	1 in z	Inter-element xy : 0.05

be macroscopic angles when aligning test boards that are spaced far apart. The alignment tolerance is a function of the device area of the VCSELs and PDs (for spatial positioning of the bars in the PGA) and the maximum deflections of the angular micropositioners used. In the experiment presented, there was a spatial positioning tolerance of approximately 15 μm (roughly three-fifths of the VCSEL/PD device area of 25 μm) for the bars in the PGA. Angular tolerance of the chip and abutted bars is approximately 100 mrad about the optical axis, while a rigorous analysis of the tip-tilt tolerance of the bars themselves was not performed.

Once oscillation is established, a detector must then be aligned in order to measure the frequency. Alignment of the detector with one of the optical channels is simplified because, with enough illumination, the detector's image is captured by the opposite camera (through the beam splitters) and superposed with that of the imaged chip corner. Thus alignment can be achieved with visual cues from a single camera image.

There are several potential concerns that arise while aligning an OERO. As discussed in Section 2, the OERO is well suited for measuring changes in device latency with respect to externally controlled variables. If the variable being controlled is optical-power throughput, care must be taken in choosing the proper mechanism for varying the power. If the source laser is multimode, then adjusting the current-drive strength to change the output power may alter the mode profile and inadvertently affect the distribution of optical power incident on the photodetector area. This effect can be avoided by maintaining a fixed current drive and inserting attenuative, nondispersive optical filters into the optical system. Adding optical elements, however, may perturb the alignment.

4. Results

The OERO described was used to measure receiver latency versus received optical power. This was achieved by varying the modulation and bias current-drive strength of the VCSELs of each chip (in a small enough range to avoid provoking multimode behavior) and observing changes in the oscillation period of the OERO. An optical power-sensing wand was inserted in the optical setup to measure the VCSEL output and to determine the throughput of the optical system, which was measured at 31%. The actual input photocurrent received by the detectors was estimated with use of the photodiode responsivity from the data sheet.

Typical measured OERO oscillation periods were from 14 to 20 ns for the circuits under test, depending on the nature of the preamplifier.⁶ Depending on the quality of the alignment, some jitter was observed on the digital scope, which was a function of received optical power. The magnitude of this jitter was estimated by observing the raw oscilloscope samples. For received optical powers of 1.5 mW, jitter comprised approximately 3–5% of the oscillation period

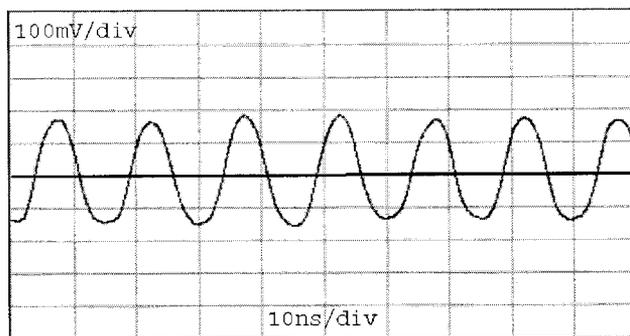


Fig. 6. Sample of an OERO sinusoid captured on the digital scope. Period of oscillation is approximately 15 ns.

(± 0.3 -ns measurement uncertainty), whereas for lower received powers near 0.5 mW the jitter was far worse, roughly 30% of the oscillation period (± 4 -ns uncertainty). Because the optical system is nondispersive, the increasing jitter can most likely be attributed to diminishing signal amplitude at the receiver. This is a familiar result from traditional electronic ring oscillators (Leeson's equation).⁸ The measurements of the oscillation period were performed with use of the averaging function of the digital scope. Averaging over 16 samples was sufficient to produce stable, consistent sinusoid traces for oscillation period measurement. An example of a sinusoidal trace detected in the experiment is presented in Fig. 6.

Of the four receiver types under test, two were based on a transimpedance (TIA) design and two were based on a common-gate amplifier (CGA) design. One of each design was implemented using dc photocurrent rejection (DCPR) designed to reduce skew in receiver arrays by stabilizing the latency over a broad range of input photocurrents. The OERO was used to demonstrate an approximate 60% reduction in skew for the CGA with use of DCPR, and a similar reduction for the TIA. A computer simulation of the oscillator is presented in Fig. 7, and a

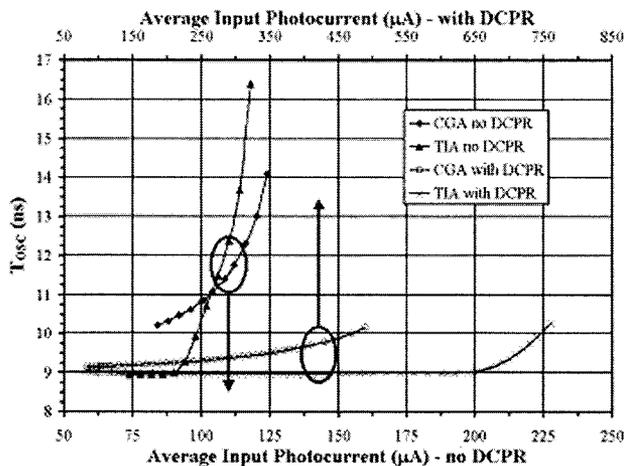


Fig. 7. Software simulation of OERO for 4 receiver types (does not account for time-of-flight and interconnect delays).

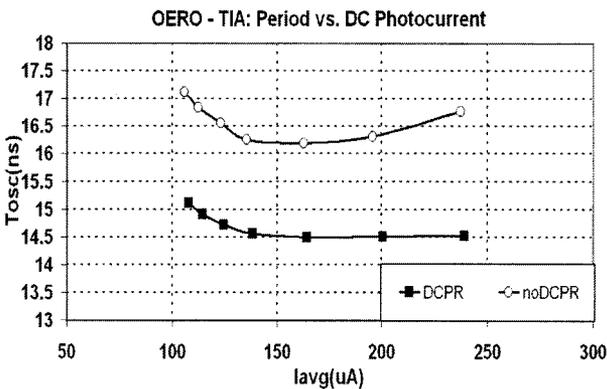
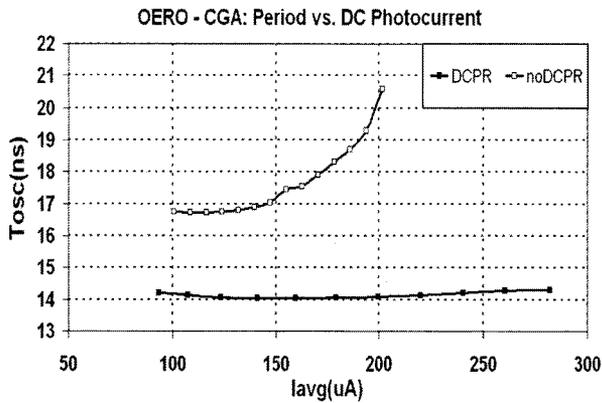


Fig. 8. OERO results for the CGA-based receivers (top) and TIA-based receivers (bottom).

sample of the results collected from the OERO is shown in Fig. 8. The experimental data indicates higher periods of oscillation owing to the existence of delays that were not accounted for in simulation (specifically, TOF and wirebond-interconnect delays).

5. Conclusion

OEROs are a novel approach to the characterization of electrical parameters of optically enabled chips. This technique is most suitable for making relative measurements of electrical parameters, such as transceiver latency with respect to externally controlled variables. OEROs have several desirable

features, including noninvasive measurement and enough versatility for a broad range of implementations.

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