0.18-μm complementary metal-oxide semiconductor push–pull vertical-cavity surface-emitting laser driver operating at 2.5 Gb/s with symmetric rising and falling edges

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A vertical-cavity surface-emitting laser (VCSEL) driver design that utilizes a novel push–pull circuit topology is described. The VCSEL driver design can provide both a current pushing and a current pulling mechanism and therefore is capable of producing symmetric rise and fall times. The design was implemented in a 0.18-μm foundry *n*-well complementary metal-oxide semiconductor technology and operates at data rates up to 2.5 Gb/s with a power consumption of 45 mW at an average optical output power of 1 mW. © 2004 Optical Society of America

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1. Introduction

The performance of very-large-scale integrated (VLSI) circuits continues to improve according to Moore's Law.[1] However, current electrical input/output (I/O) technology has not been able to keep up with improvements in chip complexity. Electrical I/O technology is limited by its high power consumption and low signal bandwidth. Several researchers have proposed optical I/O as a replacement for conventional electrical I/O for future VLSI systems.[2–4] Optical I/O has the advantage of low power consumption and high signal bandwidth. In addition, recent advances in the heterogeneous integration of vertical-cavity surface-emitting lasers (VCSELs) and photodiodes with high density VLSI electronics have shown that optical I/O can increase system connectivity.[5,6]

Low power, high-speed transmitters and receivers are key in enabling circuit connectivity technology to advance. To date, there have been a number of reports on gigabit-per-second VCSEL drivers realized in complementary metal-oxide semiconductor (CMOS).[7–10] The traditional topology of modulating the output optical power of an optical transmitter is to steer current into and out of the VCSEL. This method usually entails the placement of a current source either above or below the VCSEL in order to either source or sink current through it. In this paper, a VCSEL driver design that utilizes a novel push–pull circuit topology is proposed. This VCSEL driver provides both a current pushing and a current pulling mechanism and therefore is capable of producing symmetric rise and fall times. The advantage of this topology at high data rates (in gigabits per second), where only on–on modulation is practical owing to laser turn-on delay limitations, is how the junction capacitance of the VCSEL is rapidly charged and discharged. Current steering topologies (e.g., a conventional differential pair) provide mechanisms to either forcefully charge or forcefully discharge this capacitance, but not both. The push–pull driver topology always provides both a source and a sink for charging and discharging the VCSEL junction capacitance. The design presented here was implemented in a 0.18-μm foundry CMOS technology and was capable of a data rate of 2.5 Gb/s with a power consumption of 45 mW.

The paper is organized as follows. In Section 2,

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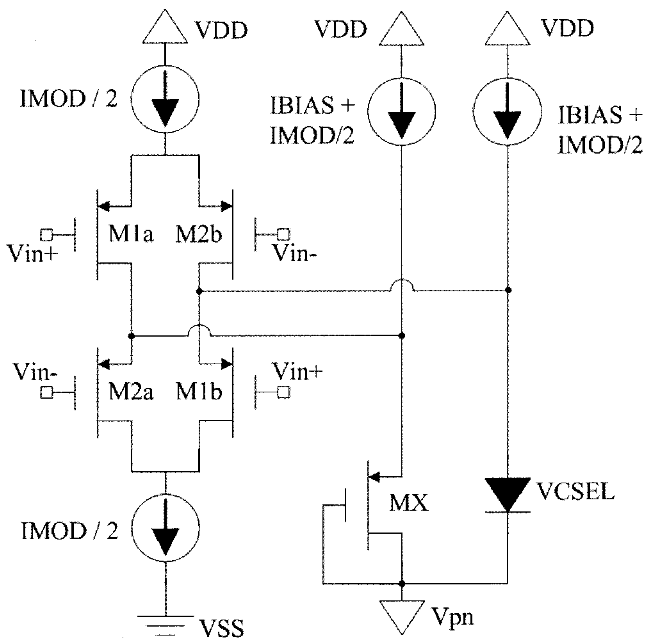

Fig. 1. Schematic of the push–pull VCSEL driver.

the design of the driver circuit is presented. Section 3 is a description of the packaging, test, and measurements of the circuits, followed by discussion and conclusions presented in Section 4.

2. Optical Transmitter Design

The optical transmitter circuit consists of an electrical receiver, a decision stage, and a VCSEL driver, driving an 850-nm VCSEL. The electrical receiver and the decision stage function as the interface between the off-chip signal and the input signal to the VCSEL driver. The electrical receiver amplifies a low-voltage differential signal generated by a high-speed data generator, which swings between 1 and 1.4 V. The electrical receiver is a fully differential amplifier with a signal gain of 11.2 dB and a simulated 3-dB frequency cutoff, f_{3dB} of 1.87 GHz. Since the input signal is expected to have a signal amplitude of 400 mV, the electrical receiver was designed for maximum speed performance at the expense of lower signal gain. The decision stage takes the signal from the electrical receiver and restores it into rail-to-rail voltage levels of 0 and 3.3 V, which are used in the next stage, the VCSEL driver. The switching threshold of the decision stage is ~1.65 V.

The VCSEL driver follows the decision stage. Figure 1 is a schematic of the push–pull circuit topology that utilized an electrically differential input scheme. One of the two differential outputs of the laser driver was connected to a VCSEL, and the other was connected to a dummy load implemented by a *p*-type metal oxide semiconductor (PMOS) transistor MX. The purpose of MX is to provide an alternate path with characteristics similar to the VCSEL for the modulation current to flow to Vpn (the *n*-contact VCSEL) when not being directed through the VCSEL. The bias current IBIAS corresponds nominally to the VCSEL threshold current. The VCSEL and the dummy load are both biased to IBIAS plus half the modulation current IMOD. This biases the VCSEL such that its output power corresponds to its average transmitted power. The transmitter circuit operates in a symmetric and balanced fashion. When Vin+ is high and Vin− is low, IMOD/2 is *pushed* into the VCSEL through M2b, corresponding to a logical high output power, and IMOD/2 is *pulled* from the dummy load through M2a. Conversely, when Vin+ is low and Vin− is high, IMOD/2 is *pulled* from the VCSEL through M1b, corresponding to a logical low output power, and IMOD/2 is *pushed* into the dummy load through M1a.

As discussed in section 1, the separate current sources allow for the junction capacitance of the VCSEL to be forcefully charged and discharged. The main disadvantage of this topology is the requirement of a stack of four transistor stacks (as shown in Fig. 1). Although such a configuration is common for high-speed circuits such as current mode logic multiplexers and flip-flops, it poses a design challenge in terms of reduced voltage headroom for the transistors in the stack - particularly for current sources in a conventional CMOS technology, where the supported supply voltage is fixed.[11] For this reason, a 3.3-V supply and 3.3-V-tolerant transistors were employed in the laser driver design. The performance of the circuit is correspondingly limited by that of the 3.3-V-tolerant transistors, and the power consumption is correspondingly larger. It is noteworthy that, in bipolar technologies, voltage headroom issues are more easily mitigated, and power and performance are more easily optimized.

The VCSEL driver was designed with PMOS transistors in order to drive the VCSEL array, which has a common *n*-contact. The dc biasing voltage at Vpn has a negative value. Hence, a negative voltage may appear at the drain–source terminals of the metal-oxide semiconductor field-effect transistor devices connected to the VCSEL. If *n*-channel metal-oxide semiconductor devices were used, forward-bias body-drain or body-source junction could result, because the body contacts of all NMOS transistors in an *n*-well CMOS technology are connected to ground. Substantial, undesirable current flow would result, thus damaging the devices. The use of PMOS devices in an *n* well prevents this from happening. The push–pull VCSEL driver described here can be readily used to drive a one or two-dimensional array of VCSELs built on a substrate with a common *n* contact. The VCSEL driver was designed to operate at data rates of up to 4 Gb/s with rise and fall times under 80 ps and to consume a maximum of 50 mW. The driver was designed to drive a VCSEL produced by Emcore Corporation (Somerset, New Jersey), which had the following characteristics: maximum data rate of 3.125 Gbps, a peak emission wavelength of 850 nm, optical rise and fall times of 60 ps, a slope efficiency of 0.45 mW/mA, a threshold current of 1.5 mA, and laser forward voltage of 1.9 V.

Fig. 2. Eye pattern of the detected optical output at 2.5 Gb/s.

3. Test and Measurements

The complete optical transmitter circuit was implemented in a 0.18-μm foundry *n*-well CMOS and fabricated by Taiwan Semiconductor Manufacturing Company (Hsinchu, Taiwan). The optical transmitter chip was placed in an 80-pin ceramic quad flat-pack chip carrier, together with a 1×4 VCSEL array provided by Emcore Corporation. Connections between the optical transmitter chip and the VCSEL were achieved by use of 1-mil gold bond wires. The chip carrier was clamped to a high-speed printed circuit board that supported high-speed testing of the chip; the 3-dB bandwidth of the packaging was specified to be 4.5 GHz and thus was more than sufficient for the purposes of testing the VCSEL driver.

A. Experimental Setup

For testing the performance of the VCSEL driver, a complete test setup was constructed, that consisted of a 10-Gb/s data generator, dc-voltage supplies, a circuit board with an optical transmitter chip clamped to it, a free-space optical system, a 12-GHz photodetector, an optical power meter, and a digital oscilloscope. The free-space optical system guides and focuses the laser beam coming out of the VCSEL on the active area of the photodetector and consists of two microscope objective lenses of 20× magnification and 0.35 numerical aperture, which are connected back to back. The first lens is placed close (at approximately 0.5 mm) to the VCSEL, taking into account the VCSEL's 28° divergence angle. The losses from the VCSEL to the photodetector are approximately 15% and are mainly caused by the multimode nature of the VCSEL and the reflection encountered at the lens surfaces. This reflection is due to the fact that the lens broadband antireflection coating is designed for wavelengths between 400 and 700 nm, instead of the 850-nm wavelength used here. A 12-GHz photodetector (with 30-ps rise–fall times) and a preamplifier assembly were used to measure the performance of the laser driver.

B. Experimental Results

A 2^{31}-1 non-return-to-zero pseudorandom bit sequence was applied to the differential inputs of the optical transmitter circuit. The eye diagram of the detected signal from the optical transmitter operating at 2.5 Gb/s is shown in Fig. 2. The measured (10%–90%) rise and fall times of the signal were 230 and 170 ps, respectively, at a data rate of 2.5 Gb/s. These measurements were obtained with the VCSEL driver operating with a 3.3-V voltage supply, and the *n* contact of the VCSEL, Vpn, biased at −0.4 V. The laser was biased 1.22 times above threshold. With these supply voltages and this bias current, the current IMOD was approximately 4.34 mA, and the power dissipation of the optical transmitter was 45 mW at 2.5 Gb/s. The optical transmitter produced an average output optical power of 1 mW. The eye-width for the 2.5-Gb/s eye diagram was estimated to be approximately 0.52 UI at an unknown bit-error rate. The experimental results obtained are close to the design target. We attribute the difference between the measured and the simulated performance to be due to several factors, including the VCSEL model used and the packaging performance.

These results compare favorably with an electrical driver in the same process technology. Specifically, a four-channel transceiver typically consumes 1.5 W at 3.125 Gb/s, or approximately 375 mW per channel for both transmit and receiver functions.[12]

4. Conclusions

A novel push–pull VCSEL driver circuit that provides both a current pushing and a current pulling mechanism has been successfully implemented in CMOS 0.18-μm technology. Experimental results showed that the laser driver operates up to a data rate of 2.5 Gb/s with a supply voltage of 3.3 V. This circuit is scalable in both data rate performance and in multielement arrays.

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