# Application of Parallel Forward-Error Correction in Two-Dimensional Optical-Data Links

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***Abstract*—We propose the use of on-chip parallel forward-error correction (FEC) to improve the performance of two-dimensional (2-D) optical-data links (2-D-ODLs). Using an optical system model that describes a 2-D-ODL, we show the merits of using the Golay code as an FEC scheme to enable the reliable operation of 2-D-ODLs in the presence of erasures [e.g., a dead laser or photodetector, a dark fiber, an alignment problem, or a fault on the application-specific integrated circuit (ASIC)]. In addition, we study the impact of using on-chip FEC in 2-D-ODLs and show that FEC can reduce the launched optical power requirements, reduce on-chip power consumption, and relax the throughput requirements of the optical system.**

***Index Terms*—Erasure, forward-error correction (FEC), Golay code, optical interconnects, optoelectronic-VLSI, packet error rate, two-dimensional optical-data link.**

## I. Introduction

PARALLEL optical interconnects (POIs) promise to deliver tremendous gains in bandwidth and interconnect density for applications such as massively parallel computing systems and telecommunication switches. At the core of any interconnect solution lies the fundamental problem of reliable transmission. Next-generation interconnect designers are running into hard limits when it comes to increasing data transmission rates and reducing errors. These two factors are typically in opposing balance: minimize bit-error rate (BER) and data rates suffer, increase transmission rates and data integrity is compromised.

The use of error-correction coding (ECC) in long-haul optical communication systems is a common approach to dealing with these problems. Forward-error correction (FEC) and automatic-repeat request (ARQ) are two techniques for performing ECC. FEC corrects errors at the receiver without the need for retransmission. The coding gain produced by ECC can be used to increase the distance between repeaters for a given BER or to increase the data rate. Two FEC approaches have been developed for long-haul optical communication systems [1]. The first is an in-band synchronous optical network/synchronous digital hierarchy (SONET/SDH) approach based on the Bose–Chaudhuri–Hocquenghem-3 code (BCH-3) [2], [3]. The specific code utilized is a shortened version of a (8191, 8152) parent code, covering 4320 information bits and utilizing 39 redundant bits. BCH-3 codes can correct up to three errors. The second approach is a digital (out-of-band) wrapper approach based on the Reed–Solomon (RS) code [4], specifically an RS(255, 239) code. The RS codes operate on symbols instead of bits. For this particular case, the symbol is an octet so the block is 255 octets in length (note that the terms "block" and "packet" will be used interchangeably throughout the rest of the paper). The payload is 239 octets, meaning that there are 16 redundant octets in the code. An RS(255, 239) code can correct up to eight symbols in error and detect (but not correct) up to 16 symbols in error.

To date, researchers have demonstrated some of the benefits of using ECC in two-dimensional (2-D) optical data links (2-D-ODLs) [5], [6]. In [5], it was demonstrated that the use of an ECC scheme based on ARQ could optimize the bandwidth of 2-D-ODLs while simultaneously decreasing the BER. However, 2-D-ODLs with large vertical-cavity surface-emitting laser (VCSEL) and photodetector (PD) arrays are likely to contain erasures due to their high sublink count. Erasures could make some ECC schemes ineffective if their error correction capability is not good enough. This is particularly true for ARQ techniques, which rely on retransmissions to correct errors. In [6], the use of RS codes in free-space optical interconnects (FSOIs) was suggested and the authors demonstrated that RS codes could facilitate an increase in both spatial density and data rate, resulting in FSOI capacity gains. Moreover, it was demonstrated that ECC could relax alignment accuracy, manufacturing uniformity, and other implementation tolerances.

Because of their inherent parallelism, 2-D-ODLs differ considerably from long-haul optical-communication systems. By transmitting data in parallel, the need for multiplexing and demultiplexing before and after transmission is reduced or eliminated. There are a number or reasons why we believe conventional error-correction techniques are not suitable for 2-D-ODLs. First, as stated in [7], conventional error-correction techniques involve decoding in a time-sequential (i.e., serial) fashion, as is shown in Fig. 1(a). In a serial implementation, one symbol of the received vector is provided as input to the decoder during each clock cycle. However, the highly parallel nature of the data transmitted over a 2-D-ODL requires an alternate solution since such a serial decoding scheme can produce a severe bottleneck in high data-rate applications. Moreover, the serial decoding scheme requires data multiplexing/demultiplexing. As depicted in Fig. 1(b), one way to

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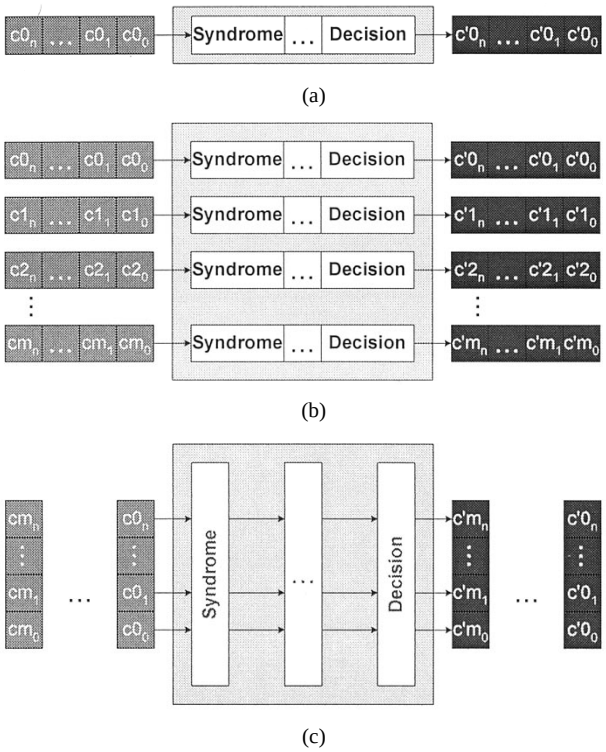


Fig. 1. Serial versus parallel error correction.

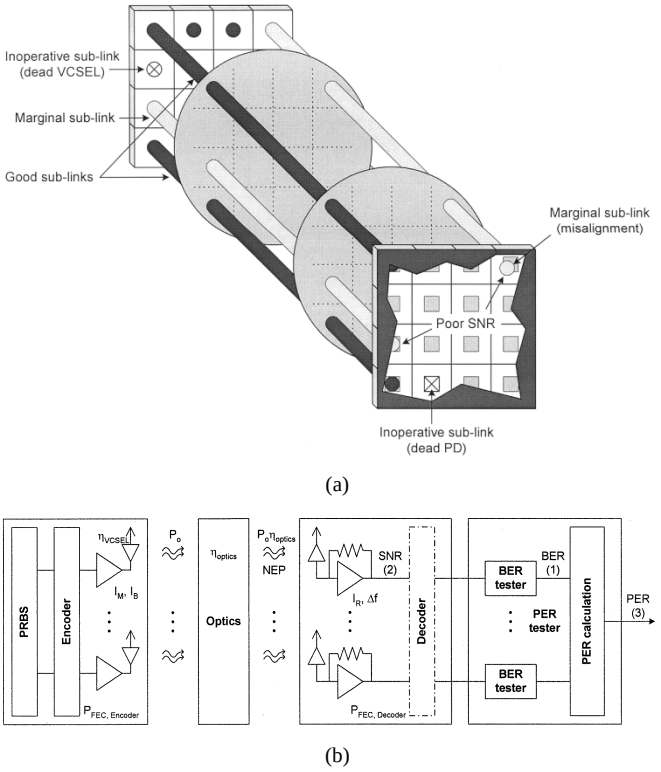


Fig. 2. (a) Sketch of a 2-D-ODL showing good sublinks, marginal sublinks, and sublinks that are inoperative. (b) Schematic representation of the 2-D-ODL with the variables in (1)–(5) annotated. The numbers in parenthesis correspond to equations in the text.

increase decoding speed within the serial paradigm is to utilize an array of serial decoders operating in parallel. Each decoder will then operate independently on separate codewords. If there are $m$ serial decoders in such an array, the aggregate decoding data rate achieved is now $m$ times that of a single serial decoder. An alternate solution is to unfold the time domain algorithm to produce a parallel pipeline decoder [see Fig. 1(c)]. This decoder receives an entire codeword at each clock cycle. Such a decoding paradigm provides to the decoder simultaneous access to all codeword symbols and can therefore yield significant savings in implementation resources as compared with the array of serial decoders [7].

Due to the long block lengths required for their implementation, the FEC techniques proposed for long-haul communication systems may not be suitable for 2-D-ODLs. The BCH-3 and the RS(255 239) codes described earlier operate on blocks of 4339 and 2040 b, respectively. A few research groups have demonstrated the integration of large arrays (over 1000 optical I/O in some cases) of VCSELs, photodetectors, and self-electrooptic effect devices (SEED) to CMOS chips [8]–[12], showing the potential for dense 2-D-ODLs. Nevertheless, conventional FEC techniques are not suitable for 2-D-ODLs that do not provide this many optical I/O. FEC schemes with a shorter block length would give more flexibility to the designer and could accommodate 2-D-ODLs of various sizes, including the smaller ones.

One more drawback to the FEC techniques used in long-haul communications is that their error-correction capability may not be sufficient for the low-yield 2-D-ODLs considered in our model. To date, over 5760 multiple quantum-well (MQW) detector/modulator devices have been integrated onto a single CMOS IC with a device yield exceeding 99.95% [13]. On the other hand, the technology is not as mature for the integration of large VCSEL arrays onto CMOS chips. The yield after bonding and packaging can be as low as 96% in this case [14]. Clearly, the error-correction capability of the RS(255, 239) code, with 64 bits out of 2040 $(\sim 3\%)$ in the best case (assuming perfect clustering of the errors), would fail to provide a performance improvement under such low yield conditions. One workaround is to use an RS code with a shorter block length but a comparable error-correction capability. It then becomes possible to use many small RS codecs (encoder/decoder pairs) to cover the array as opposed to one big RS(255, 239) codec. Note that the number of errors that can be corrected may depart from the number assumed initially if the errors are not spread out evenly among the decoders. Moreover, codes with a smaller block length have a lower information rate for a given error-correction capability, but as we will see later, a good error-correction capability can make up for a low information rate through the concept of coding gain.

Our analysis builds on the work of [5] and [6] by adding erasures and marginal sublinks (both terms will be defined in Section II below) to our 2-D-ODL model. We demonstrate that an ECC scheme based on FEC can 1) reduce the required laser-launched power to achieve a given BER; 2) maintain a target BER of $10^{-15}$ in the presence of erasures; 3) reduce the on-chip power consumption; and 4) relax optical-system throughput requirements. The rest of the paper is organized as follows. In Section II, we will describe the 2-D-ODL model that we considered in our analysis. We will introduce the RS(15, 9), RS(15, 7), BCH(31, 16), BCH(15, 7), and Golay codes [15] as potential candidates for parallel on-chip FEC. These codes were se-

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TABLE I
LIST OF POTENTIAL FEC CODES FOR ON-CHIP FEC IN 2-D-ODLS. FOR THE SAKE OF COMPARISON, AN ARRAY OF $16 \times 16$ OPTICAL I/O IS ASSUMED. THE NUMBER OF CODECS THAT CAN FIT IN THE ARRAY IS OBTAINED BY TAKING THE FLOOR OF $256/n$. $n$ IS THE NUMBER OF BITS PER BLOCK, $k$ IS THE NUMBER OF INFORMATION BITS (PAYLOAD), $t$ IS THE NUMBER OF ERRORS THAT CAN BE CORRECTED, AND $R$ IS THE INFORMATION RATE $(k/n)$. THE TOTAL NUMBER OF ERRORS THAT CAN BE CORRECTED $(T)$ ASSUMES A RANDOM DISTRIBUTION OF THE ERRORS ACROSS THE ARRAY SO THAT EACH DECODER HAS TO HANDLE THE SAME NUMBER OF ERRORS

| | Golay (24,12) | RS(15,9) | RS(15,7) | BCH(15,7) | BCH(31,16) |
|---|---|---|---|---|---|
| n | 24 | 60 | 60 | 15 | 31 |
| k | 12 | 36 | 28 | 7 | 16 |
| R | 50% | 60% | 47% | 47% | 52% |
| t | 3 | 3 | 4 | 2 | 3 |
| # codecs | 10 | 4 | 4 | 17 | 8 |
| T | 30/240 | 48/240 (Best case)<br>12/240 (Worst case) | 64/240 (Best case)<br>16/240 (Worst case) | 34/255 | 24/255 |
| Minimum yield requirement | 87.5% | 80% (Best case)<br>95% (Worst case) | 73.3% (Best case)<br>93.3% (Worst case) | 86.7% | 90.6% |
| Ref. for decoder | This work (based on [16]) | [7] | | | |
| Technology | CMOS 0.18 μm | CMOS 2 μm | | | |
| Decoder latency (d) | 3.33 ns | 24.3 ns | | | |
| Decoder aggregate throughput (# codecs × k × 1/d) | 36 Gb/s | 5.9 Gb/s | | | |
| Decoder complexity (1 decoder) | 16,475 transistors | 33,000 transistors | | | |
| Decoder area (1 decoder) | $200 \times 200$ μm$^2$ | N/A | | | |
| Power dissipation (1 decoder) | 37.41 mW @ 300 Mb/s | N/A | | | |

lected because they all have a short block length and a good error-correction capability. The emphasis will be placed on the Golay code because a fast, area-efficient, purely combinational parallel decoder was readily available from the literature [16]. In Section III, numerical results will be presented and analyzed. Section IV is a discussion and conclusion section.

## II. SYSTEM MODEL

Our analysis will be performed on 2-D-ODLs such as the one shown in Fig. 2(a). For clarity, only 16 sublinks are shown in the picture (four of which are transmitting data). However, our analysis holds for a 2-D-ODL of any size. Arrays of VCSELs and PDs are heterogeneously integrated with CMOS chips [12]. Throughout this work, a transmitter will refer to a VCSEL and its driving circuit, and a receiver will refer to the PD, the transimpedance amplifier (TIA), and the postamplifier. Furthermore, FEC will specifically refer to the use of the Golay code and the terms frequency and data rate (or bit rate) will be used interchangeably. The optical interconnect can either use free-space optics or guided-wave optics, but the later case will be assumed to simplify the analysis in Section III.

Fig. 2(a) depicts a schematic of a 2-D-ODL showing three types of sublinks: good sublinks, marginal sublinks and inoperative sublinks. Good sublinks have a low BER, being subject only to statistically unavoidable random errors arising from, for example, noise in the receiver or intersymbol interference. Marginal sublinks have a BER higher that the average BER due to a poor SNR at the receiver output. There are a number of causes of poor SNR: an abnormal performance degradation of a VCSEL or PD over time, process variations on the ASIC, the VCSEL and PD arrays, and power throughput nonuniformity in the optical system due to aberrations or misalignment [17]. Inoperative sublinks are permanent sublink failures that can be due to, for example, a dead VCSEL, a dead PD, a dark fiber, a completely misaligned link, or a fault on the ASIC. We will refer to inoperative sublinks as erasures throughout the rest of the paper.

The FEC codes initially considered in our model are listed in Table I. The codes, although very different, share a few similarities. First, they all have a short block length compared to the RS and BCH codes used in long-haul optical-communication systems. As we saw earlier, short codeword lengths are desirable for packet data communications in which data is transmitted in parallel. Second, the FEC codes considered all have a good error-correction capability, which makes up for their low information rate (less than 50% in certain cases). The Golay and BCH codes have in common that they operate on bits, whereas RS codes operate on symbols [a symbol is composed of 4 bits for the RS(15, 9) and RS(15, 7) codes]. The number of symbols that a given RS codec can correct is constant, but the number of bits depends on the spatial distribution of the errors. If the errors are clustered, then the RS codes will offer the best error-correction capability of all codes listed in Table I. On the other hand, if the errors spread out randomly across the array, then the RS codes will perform poorly. Third, because latency is to be minimized in 2-D-ODLs, we only considered FEC codes for which efficient decoders existed and therefore could be implemented on the same chip as the transceivers and the other digital functions. On-chip FEC has the added advantage of reducing pin count, which may be a bottleneck for large optoelec-

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tronic-VLSI (OE-VLSI) chips. All codes listed in Table I are linear and block-based, which means that efficient decoding algorithms exist for them.

Codes not listed in Table I include the Viterbi codes [18], the Turbo codes [19], and the Hamming codes [20]. The Viterbi codes belong to the class of convolutional codes. They differ from block-based codes in that they require memory for decoding, making them less attractive. Turbo codes achieve performance near the Shannon limit. The iterative algorithm is one of the key components in turbo decoding, providing significant implementation challenges. Iterative decoding trades off latency for error-correcting performance and should be avoided in applications requiring low latency. The last codes to be considered were the Hamming codes. Despite the existence of very efficient decoders, we concluded that their limited error-correction capability was insufficient for a 2-D-ODL.

Without loss of generality, we chose the Golay code to model the FEC block in our analysis. In particular, an area-efficient decoding algorithm proposed by Cao [16] was selected. The (24, 12) extended Golay code is a half-rate code that can correct and detect three and four errors out of a 24-bit codeword, respectively. The 12 extra bits are used at the receiver in an attempt to correct errors that may have occurred during transmission. Performance figures of the Golay encoder and decoder blocks will be given in Section III. In Section IV, we will compare our parallel Golay decoder to the parallel RS(15, 9) decoder proposed in [7].

In the following analysis, the target packet error rate (defined below) is $10^{-15}$. The target aggregate bandwidth is 10.8 Gb/s and, as is indicated in Table II, every 2-D-ODL considered has enough sublinks and a sufficient data rate per sublink to support this aggregate bandwidth.

### A. Bit-Error-Rate Versus Signal-to-Noise Ratio

We will consider a 2-D-ODL that uses the direct-detection (DD) modulation scheme. In the DD scheme, the absence of optical power denotes a logical 0 and the presence of optical power denotes a logical 1. The basic BER of an optical data link that uses the DD modulation scheme, denoted $\mathrm{BER_{DD}}$, is given by [21], [22]

$$\mathrm{BER_{DD}} = \frac{1}{2}\left[1 - erf\left(\frac{\sqrt{\mathrm{SNR}}}{2\sqrt{2}}\right)\right] = \frac{1}{2}\left[erfc\left(\frac{\sqrt{\mathrm{SNR}}}{2\sqrt{2}}\right)\right] \quad (1)$$

where the SNR is measured at the receiver output, as shown in Fig. 2(b).

The noise at the receiver output is comprised of two components. The first component is the detector-amplifier thermal noise characterized by a noise-equivalent power (NEP) referred to the optical domain [22]. The advantage of specifying NEP for a receiver is that it can be used to estimate the optical power needed to obtain a specific value of SNR if the bandwidth f is known [see (2)]. The second component is simultaneous switching noise and electrical crosstalk, which are generated from neighboring receivers, digital circuitry, and on-chip transmitter drivers, attacking the receiver output via the power and ground rails and through the substrate [23]. It is well known that the effects of switching noise will dominate the effects of thermal noise in OE-VLSI chips [24]–[27]. To the authors' knowledge, however, there exists no deterministic/statistical approach to modeling switching noise. Thus, we have used a deterministic modeling approach following [5], [6], where thermal noise is assumed to be the dominant noise source. The effects of neglecting switching noise in the analysis that follows will be discussed in Section IV.

We assume that the optical transmission is through guided-wave optics, for which the optical cross talk is negligible. Under these assumptions, the SNR at the receiver output can be approximated using the power incident on the photodiode [22]

$$\mathrm{SNR} = \frac{P_o \eta_{\mathrm{optics}}}{\mathrm{NEP}\sqrt{f}} \quad (2)$$

where $P_o$ is the average VCSEL launched power, $\eta_{\mathrm{optics}}$ is the throughput of the optics, and $f$ is the bandwidth of the receiver. Note that the SNR is a function of the PD responsivity through the NEP term [22]. This definition of SNR ignores intersymbol interference, which increases the noise at high frequencies. However, at the data rates considered ($<$450 Mb/s), intersymbol interference should not be an issue and was neglected. Throughout our discussion, we will assume an NEP of 0.3 nW/Hz$^{1/2}$, as in [5], [6]. This value is compatible with simple receiver designs that can achieve a $\mathrm{SNR} = 10$ with 50 $\mu$W of optical power over a bandwidth of 250 MHz in the absence of intersymbol interference [28].

### B. Packet-Error Rate Versus Bit-Error Rate

Because data is transmitted in parallel, the figure of merit that we will use to compare the performance of different 2-D-ODLs is the packet-error rate (PER), defined as

$$\mathrm{PER_t} = \sum_{z=t+1}^{n} P(z) \cong P(t+1) \text{ for } p_e \ll 1, \text{ where}$$
$$P(t) = \binom{n}{t} p_e^t (1-p_e)^{n-t} \quad (3)$$

$P(t)$ in (3) gives the probability of finding $t$ errors out of an $n$-bit packet given the raw bit-error rate (BER) of each individual sublink. The raw BER is the probability of error $(p_e)$ of a sublink. The PER as defined in (3) states that the probability of a packet error using an FEC scheme capable of correcting $t$ errors is the sum of the probabilities of finding $(t+1)$ to $n$ errors out of the $n$-bit packet. This definition assumes that the errors are statistically independent and that all the sublinks except the erasures have the same raw BER (i.e., we assume no marginal sublinks). Our analysis will therefore consider random errors from good sublinks and erasures from inoperative sublinks. Because our analysis will be based on the use of the Golay code, for which $t = 3$ in (3), the acronym PER will refer to $\mathrm{PER_3}$ throughout the rest of the paper.

### C. On-Chip Power Consumption

The following two formulas will be used to compare the on-chip power consumption of a 2-D-ODL without FEC to that of a 2-D-ODL with FEC

$$P_{\mathrm{on-chip,no\ FEC}} = K\left[I_B + I_{M,\mathrm{no\ FEC}} + I_R(f)\right] V_{\mathrm{DD}} \quad (4)$$

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TABLE II
VALUES USED FOR THE VARIABLES IN (4) AND (5). $K$ IS OBTAINED BY DIVIDING 10.8 GB/S BY THE DATA RATE. DIVIDING $K$ BY 12 (THE NUMBER OF INFORMATION BITS FOR THE GOLAY CODE) GIVES THE NUMBER OF ENCODER/DECODER PAIRS. THE ENCODER AND DECODER BLOCKS WERE SYNTHESIZED IN 0.18-$\mu$m CMOS. THE RECEIVER [12]WAS DESIGNED IN 0.35-$\mu$m CMOS AND $I_R$ HAS THEREFORE BEEN SLIGHTLY OVERESTIMATED IN OUR ANALYSIS

| Data rate (Mb/s) | K | # enc/decode pairs | Encoder power (mW) | Decoder power (mW) | Sum (mW) | Area (for one pair) ($\mu m^2$) | Total area for FEC block ($\mu m^2$) | $P_{FEC}$ (mW) | $I_R$ (mA) |
|---|---|---|---|---|---|---|---|---|---|
| 50 | 216 | 18 | 0.16 | 7.92 | 8.08 | 205 × 205 | 867 × 867 | 145.45 | 2.155 |
| 75 | 144 | 12 | 0.23 | 11.60 | 11.83 | 205 × 205 | 708 × 708 | 142.00 | 2.165 |
| 100 | 108 | 9 | 0.31 | 15.14 | 15.45 | 205 × 205 | 614 × 614 | 139.09 | 2.175 |
| 150 | 72 | 6 | 0.46 | 21.54 | 22.00 | 205 × 205 | 501 × 501 | 131.97 | 2.195 |
| 180 | 60 | 5 | 0.54 | 25.06 | 25.60 | 205 × 205 | 457 × 457 | 128.02 | 2.208 |
| 225 | 48 | 4 | 0.66 | 29.97 | 30.63 | 205 × 205 | 409 × 409 | 122.53 | 2.228 |
| 300 | 36 | 3 | 0.87 | 37.41 | 38.28 | 205 × 205 | 354 × 354 | 114.84 | 2.261 |
| 450 | 24 | 2 | 1.30 | 56.17 | 57.47 | 286 × 286 | 404 × 404 | 114.94 | 2.323 |

$$P_{\text{on-chip, with FEC}} = \frac{K}{R}\left[I_B + \frac{I_{M,\text{no FEC}}}{\alpha(f)} + I_R(f)\right] V_{\text{DD}} + P_{\text{FEC}}(f). \quad (5)$$

Fig. 2(b) shows a schematic representation of the 2-D-ODLs considered in our analysis with the variables in (4) and (5) included as annotations. For the purposes of calculation and comparison, we assume that the FEC block and the transceivers (transmitters + receivers) are implemented in a commercial 0.18 $\mu$m CMOS technology, for which $V_{\text{DD}} = 1.8$ V. $I_B$ and $I_M$ model the bias and modulation currents of the VCSEL driver, respectively. $I_R$ models the current supplied to the receiver. The receiver current and the power consumption of the FEC block are both frequency dependent, as will be seen in Section III. $K$ represents the number of sublinks, each operating at a data rate $f$ necessary to achieve an aggregate bandwidth of $K \times f = 10.8$ Gb/s. $R$ represents the information rate of the Golay code and has a value of 0.5. Assuming the sublink data rate $f$ is held constant, adding FEC requires doubling the number of sublinks if the aggregate bandwidth is to be kept constant. $I_{M,\text{no FEC}}/\alpha(f)$ represents the (ideally smaller) modulation current required for a 2-D-ODL with FEC to achieve a PER of $10^{-15}$. $\alpha(f)$ is therefore the factor by which the modulation current can be reduced as a result of using FEC.

## III. NUMERICAL RESULTS AND ANALYSIS

In this section, we will present case analyzes using the 2-D-ODL model described in Section II. To perform the analysis, typical values for all variables in (4) and (5) were required. In order to model the Golay encoder and decoder described in [16], we synthesized them in a 0.18-$\mu$m CMOS technology using the Synopsys synthesis tool. For a decoder with a maximum propagation delay of 3.25 ns (corresponding to a data rate of approximately 300 Mb/s), the area predicted was $200 \times 200$ $\mu m^2$. For a maximum propagation delay of 2.16 ns (corresponding to a data rate of approximately 450 Mb/s), the predicted area doubled to $283 \times 283$ $\mu m^2$. The encoder is much simpler than the decoder and the design could be synthesized in an area of $42.72 \times 42.72$ $\mu m^2$ with a maximum propagation delay of 1.12 ns, corresponding to a data rate of approximately 900 Mb/s. Clearly, the decoder is the bottleneck in the encoder/decoder pair. For the sublink data rates considered (see Table II), the maximum number of codecs needed to sustain an aggregate bandwidth of 10.8 Gb/s is 18. Even with this many codecs, the predicted total area of the FEC block was $867 \times 867$ $\mu m^2$. This is less than 1 $mm^2$ for

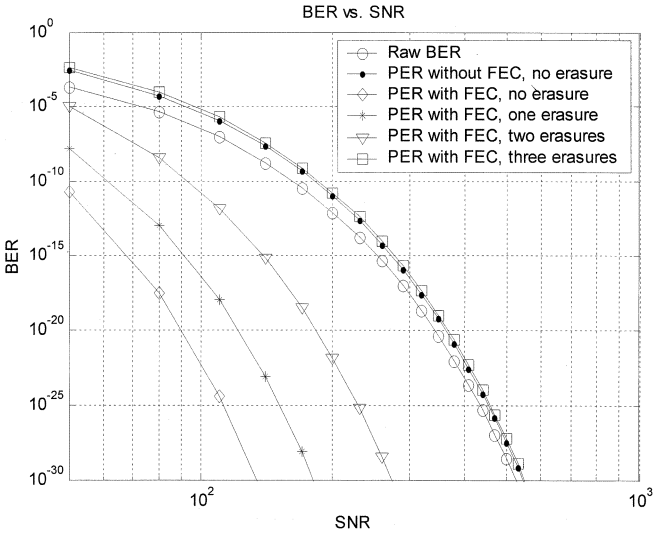


Fig. 3. BER as a function of the signal-to-noise current ratio at the receiver output.

TABLE III
SNR REQUIRED TO ACHIEVE A BER/PER OF $10^{-15}$

| Case | SNR | SNR (dB) |
|---|---|---|
| 1. Raw BER | 253 | 24.0 |
| 2. PER without FEC, no erasure | 272 | 24.3 |
| 3. PER with FEC, no erasure | 69 | 18.4 |
| 4. PER with FEC, 1 erasure | 92 | 19.6 |
| 5. PER with FEC, 2 erasures | 139 | 21.4 |
| 6. PER with FEC, 3 erasures | 277 | 24.4 |

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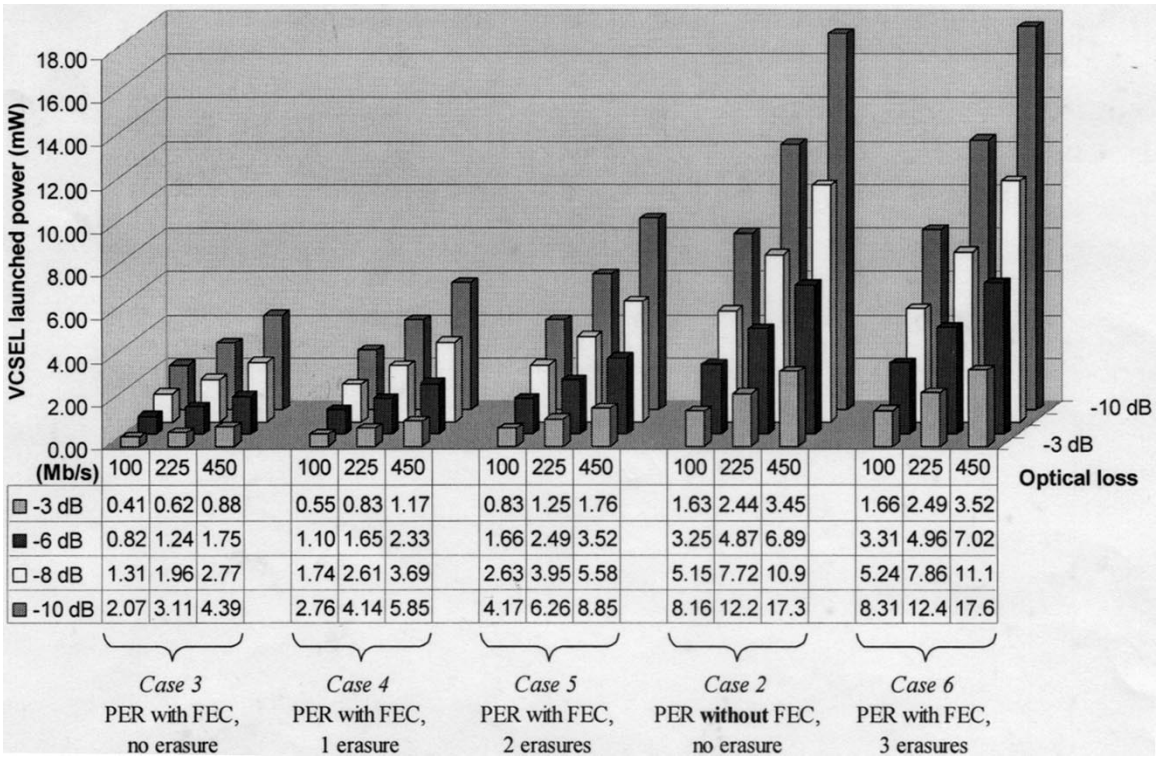


| (Mb/s) | 100 | 225 | 450 | 100 | 225 | 450 | 100 | 225 | 450 | 100 | 225 | 450 | 100 | 225 | 450 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| -3 dB | 0.41 | 0.62 | 0.88 | 0.55 | 0.83 | 1.17 | 0.83 | 1.25 | 1.76 | 1.63 | 2.44 | 3.45 | 1.66 | 2.49 | 3.52 |
| -6 dB | 0.82 | 1.24 | 1.75 | 1.10 | 1.65 | 2.33 | 1.66 | 2.49 | 3.52 | 3.25 | 4.87 | 6.89 | 3.31 | 4.96 | 7.02 |
| -8 dB | 1.31 | 1.96 | 2.77 | 1.74 | 2.61 | 3.69 | 2.63 | 3.95 | 5.58 | 5.15 | 7.72 | 10.9 | 5.24 | 7.86 | 11.1 |
| -10 dB | 2.07 | 3.11 | 4.39 | 2.76 | 4.14 | 5.85 | 4.17 | 6.26 | 8.85 | 8.16 | 12.2 | 17.3 | 8.31 | 12.4 | 17.6 |

Fig. 4. VCSEL launched-power requirement to achieve a PER of $10^{-15}$ as a function of data rate, optical loss, and number of erasures. The corresponding SNR requirement for each case can be found in Table III.

an aggregate bandwidth of 10.8 Gb/s, and we therefore believe that the Golay code is suitable for on-chip FEC.

Table II shows the power consumption of the FEC block $(P_{\mathrm{FEC}})$ at various data rates. Note that the power consumption of the encoder and decoder blocks taken individually follow the rule $P_d = C_L V_{\mathrm{DD}} f_p$ [29], where $P_d$ is the dynamic power consumption, $C_L$ is the capacitive load, $V_{\mathrm{DD}}$ is the supply voltage, and $f_p$ is the frequency of operation. On the other hand, $P_{\mathrm{FEC}}$ is not proportional to the data rate because the number of codecs is reduced as the data rate increases.

Referring to Table II, the current drawn from the power supply $(I_R)$ was obtained from the simulation of the single-ended receiver described in [12]. The receiver was designed in 0.35 $\mu$m CMOS, whereas our analysis considers 0.18 $\mu$m CMOS. Because the current drawn from the power supply is expected to decrease with the improvement of CMOS technology, the variable $I_R$ in (4) and (5) was slightly overestimated. $V_{\mathrm{DD}}$ was assumed to be 1.8 V, which is the typical power supply voltage in 0.18 $\mu$m CMOS. We assumed VCSELs with a threshold current of 1.5 mA and a bias current equal to the threshold current. Because the Golay code is a half-rate code, the variable $R$ in (5) was set to 0.5 throughout the simulations. Variable $K$ depends on the data rate of the sublinks (see Table II).

### A. SNR Requirement to Achieve a PER of $10^{-15}$

Using (1), the raw BER was plotted against SNR and is shown in Fig. 3. The PER for five other cases was plotted in the same figure using (3). The second case of interest is without FEC and no erasures. At any given SNR, the PER is greater than the raw BER of each individual sublink. This can be explained by the fact that any one of the 12 sublinks can cause a packet error. The SNR required to achieve a PER of $10^{-15}$ is 24.3 dB (see Table III). In the third case, with FEC and no erasures, the SNR can be brought down to 18.4 dB, corresponding to a 5.9-dB coding gain at a PER of $10^{-15}$. In cases 4 to 6, a 24-bit ODL with 1, 2, and 3 erasures requires an SNR of 19.6, 21.4, and 24.4 dB, respectively. It should be noted that for a given SNR, the PER for case 6 is slightly higher than in case 2. This is due to the fact that the probability of finding one error out of a 21-bit packet is higher than finding one error in a 12-bit packet. Note that only 21 bits are considered in the calculation of the PER in case 6. The decoder corrects the three erasures and therefore, the PER becomes the probability of finding one error out of a 21-bit packet. The same discussion applies to cases 4 and 5, where the PER is calculated on 23 and 22-bit packets, respectively.

### B. VCSEL Launched Power Requirement

Fig. 4 shows the VCSEL launched power required to achieve a PER of $10^{-15}$ under various conditions. The VCSEL launched power is tabulated in the figure as a function of data rate, optical loss and number of erasures. Cases 2 to 6 of Section III-A are considered here. The cases were ordered from left to right according to their launched power requirement. For the same set of conditions, the 2-D-ODL that will require the lowest VCSEL launched power is the one with FEC and no erasures. For example, consider a 2-D-ODL operating at 225 Mb/s/sublink and having an optical loss of $-6$ dB (which corresponds to an optical throughput of about 25%). The VCSEL launched powers for cases 2 and 3 are 4.87 mW and 1.24 mW, respectively. FEC therefore reduces the required VCSEL launched power by a factor of 3.9 when there are no

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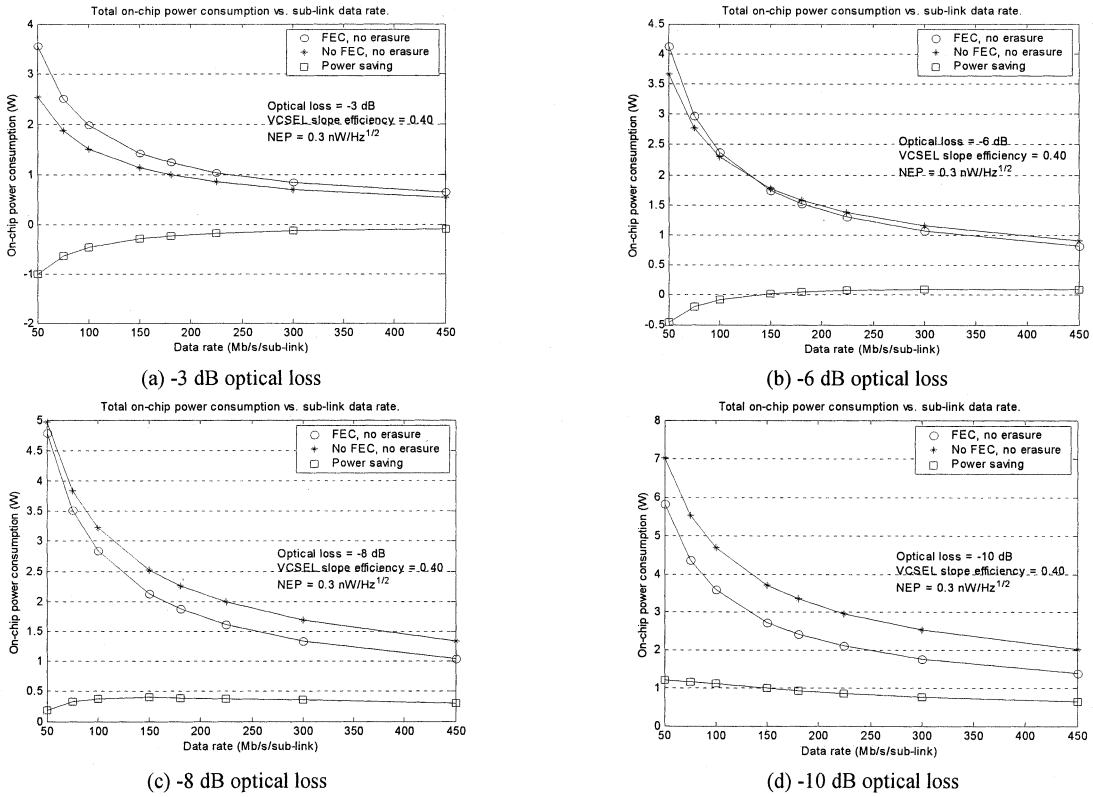


Fig. 5. On-chip power consumption for two 2-D-ODLs with no erasures. One 2-D-ODL has FEC and the other one does not. The NEP and the VCSEL slope efficiency were assumed to be 0.3 nW/Hz$^{1/2}$ and 0.4 mW/mA, respectively.

erasures. Moreover, the application of FEC to a 2-D-ODL with as many as two erasures decreases the VCSEL launched power by a factor of almost 2 (4.87 mW versus 2.49 mW) while maintaining a PER of $10^{-15}$. Because the SNR requirement for cases 2 and 6 is almost the same (see Table III), the VCSEL launched powers are comparable.

The required VCSEL launched power increases with frequency (see Fig. 4). This can be explained by (2), from which it is clear that the VCSEL launched power must increase proportionally to the square root of frequency in order to maintain a constant SNR and PER. Fig. 4 also suggests that the launched power increases with optical loss. This is also in accordance with (2), which indicates that the VCSEL launched power must increase proportionally to the optical throughput to maintain a constant SNR. At high data rates or for high optical losses, a point is reached where the required VCSEL launched power is not practical or realistic anymore. For example, consider the 2-D-ODLs of cases 2 and 5 in Fig. 4. Assuming that the 2-D-ODLs use VCSELs having a maximum optical output power of 5 mW, Fig. 4 says that there are certain data rates or optical losses that would require too large a VCSEL launched power to maintain the PER below $10^{-15}$. The 2-D-ODL of case 2 (no FEC) will not be able to maintain a PER of $10^{-15}$ if the optical loss is $-8$ dB. However, provided that the data rate is 225 Mb/s or less, the 2-D-ODL of case 5 (with FEC) will be able to maintain a PER of $10^{-15}$ under the same optical loss condition. Additionally, the 2-D-ODL of case 5 is able to handle two erasures.

In summary, our analysis thus far suggests three advantages regarding the use of FEC: 1) the incorporation of FEC will permit a 2-D-ODL to be operationally successful in the presence of erasures; 2) FEC leads to a reduction of the VCSEL launched power; and 3) FEC leads to an acceptable increase of the optical system insertion losses, which in turn relaxes packaging and alignment tolerances.

### C. On-Chip Power Consumption

We saw in Section III-B that FEC can significantly decrease the required VCSEL launched power to achieve a given PER. In this section, we will show that FEC can also decrease, in some cases, the on-chip power consumption. This is perhaps counterintuitive, considering that FEC doubles the number of sublinks necessary to support a given aggregate bandwidth (assuming the sublink data rate is held constant). A reduction of the required VCSEL launched power due to FEC can counter balance or even offset the power consumed by the FEC block and the additional transceivers, leading to a reduction in the overall power consumption.

Using (4) and (5), the on-chip power consumption of 2-D-ODLs with no erasures (cases 2 and 3) were plotted in Fig. 5. Table IV presents a greater subset of the results. Fig. 5(a) shows that when the optical loss is $-3$ dB, a 2-D-ODL with FEC consumes more power than a 2-D-ODL without FEC at any data rate, for a negative power savings. From Table IV, the power penalty is 464 mW, 185 mW, and 96 mW for data rates of

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TABLE IV
ON-CHIP POWER CONSUMPTION DIFFERENCE BETWEEN A 10.8 GB/S 2-D-ODL WITH FEC AND A 2-D-ODL WITHOUT FEC AND NO ERASURE. A POSITIVE NUMBER MEANS A POWER SAVING. THE CASES REFER TO THE CASES OF TABLE III

| Case | Data rate (Mb/s) | Optical loss -3 dB | -6 dB | -8 dB | -10 dB |
|---|---|---|---|---|---|
| *Case 2* PER without FEC, no erasure | 100 | 0 | 0 | 0 | 0 |
| | 225 | 0 | 0 | 0 | 0 |
| | 450 | 0 | 0 | 0 | 0 |
| *Case 3* PER with FEC, no erasure | 100 | -0.464 | -0.076 | 0.379 | 1.100 |
| | 225 | -0.185 | 0.074 | 0.377 | 0.858 |
| | 450 | -0.096 | 0.087 | 0.301 | 0.641 |
| *Case 4* PER with FEC, 1 erasure | 100 | -0.598 | -0.343 | -0.044 | 0.430 |
| | 225 | -0.274 | -0.104 | 0.095 | 0.411 |
| | 450 | -0.159 | -0.039 | 0.102 | 0.325 |
| *Case 5* PER with FEC, 2 erasures | 100 | -0.871 | -0.888 | -0.909 | -0.941 |
| | 225 | -0.456 | -0.468 | -0.481 | -0.503 |
| | 450 | -0.288 | -0.297 | -0.306 | -0.321 |
| *Case 6* PER with FEC, 3 erasures | 100 | -1.674 | -2.490 | -3.448 | -4.965 |
| | 225 | -0.992 | -1.536 | -2.174 | -3.186 |
| | 450 | -0.667 | -1.052 | -1.503 | -2.218 |

100, 225, and 450 Mb/s/sublink, respectively. A $-3$ dB optical loss is a relatively conservative number and therefore, optical losses of $-6$, $-8$, and $-10$ dB were considered in Fig. 5(b)–(d), respectively. For a $-6$ dB optical-power loss, FEC will provide power savings for data rates above approximately 150 Mb/s. From Table IV, this power saving is 74 mW at 225 Mb/s and 87 mW at 450 Mb/s. Furthermore, as the optical loss increases, the break-even data rate decreases. For an optical loss of $-8$ dB or more, FEC reduces the power consumption of a 2-D-ODL at all data rates considered [see Fig. 5(c) and (d)].

In terms of PER, the overall performance of a 2-D-ODL is determined by its worst sublink. This is so, because an error in any one of the sublinks transmitting in parallel will cause a packet error. A 2-D-ODL with no FEC and only one erasure will therefore fail to provide a PER of $10^{-15}$. On the other hand, a 2-D-ODL with FEC will be able to tolerate as many as three erasures out of a 24-bit packet before it fails to provide a PER of $10^{-15}$. We explore this further by comparing the power consumption of a 2-D-ODL without FEC (case 2) to the power consumption of a 2-D-ODL with FEC and one (case 4), two (case 5) or three (case 6) erasures. In case 2, a 2-D-ODL with absolutely no defect is needed because no erasure can be tolerated. In cases 4 to 6, a less than perfect 2-D-ODL is acceptable since three erasures can be tolerated out of 24 sublinks. Fig. 6(a) shows that the 2-D-ODL with one erasure gives a power saving relative to the 2-D-ODL without FEC and no erasures—assuming a data rate greater than 150 Mb/s and an optical loss of $-8$ dB. As is shown in Fig. 6(b), the power saving is greater for a $-10$ dB optical loss. Fig. 6(c) shows that we stop having a power saving for the two or three-erasure cases (cases 5 and 6), only case 5 is shown in the figure. With two erasures and an optical loss of $-10$ dB, the on-chip power penalty is 503 mW and 321 mW (see Table IV) at data rates of 225 and 450 Mb/s, respectively. Although there is an increase in the on-chip power consumption, this is acceptable since the 2-D-ODL can operate in the presence of erasures. Without FEC and in the presence of an erasure, the 2-D-ODL would have an unacceptable PER under any circumstance.

## IV. DISCUSSION AND CONCLUSION

Throughout Section III, we have assumed a thermal noise-limited system. Our model could be made more accurate by including the effects of switching noise, which was discussed in Section II. Unfortunately, to the knowledge of the authors, no closed-form expression of the form of (2) exists to relate switching noise to SNR. We nevertheless qualitatively predict the impact of switching noise on the results presented in Section III. First, adding switching noise to our analysis would not change the SNR requirements of Table III since the SNR is determined from the target PER of the 2-D-ODL [see (1)].

Second, we expect that the denominator in (2) would not have a simple $\sqrt{f}$ dependence. For a given number of sublinks, the amount of switching noise is expected to increase with frequency. However, as $f$ goes up in our model, the array size goes down (see Table II) and switching noise is expected to go down accordingly. If $f$ becomes large enough, it is conceivable that switching noise becomes negligible compared to thermal noise. Despite the lack of a formula similar to (2) for switching noise-limited systems, we can safely assume that, under the same incident-optical power on the receivers, the SNR of a switching noise-limited system will be worse than that of a thermal noise-limited system. This in turn will cause an increase in the VCSEL launched-power requirement and an upward shift of the curves in Figs. 5 and 6. Switching noise, when dominant, would therefore increase on-chip power consumption. It is not clear, however, how the crossing points in Figs. 5(b) and 6(a) would be affected by switching noise.

In Section II, we proposed a few alternatives to the Golay codes for use in 2-D-ODLs. We wish to draw the reader's attention to the RS(15, 9) code because a parallel architecture already exists for this decoder [7]. The Golay decoder employed in this work is compared to the parallel RS decoder in Table I. Since the two decoders handle different block lengths, we assumed an array of $16 \times 16$ VCSELs/PDs and calculated the total aggregate throughput using the number of decoders that could fit in the array. The RS decoder was implemented in CMOS 2 $\mu$m. When the propagation delay is scaled down linearly for appropriate comparison with the Golay decoder, we obtain an aggregate data rate of 65.8 Gb/s. The RS(15, 9) would therefore provide more aggregate bandwidth than the Golay decoder when normalized to the number of sublinks available. This is mainly due to the fact that the RS(15, 9) code has a higher information rate than the Golay code. On the other hand, the number of transistors of the RS(15, 9) decoder is more than twice the number of transistors of the Golay decoder. Since area is critical for on-chip FEC, the Golay decoder would have an advantage on the RS decoder with respect to area. One last point worth noting is that

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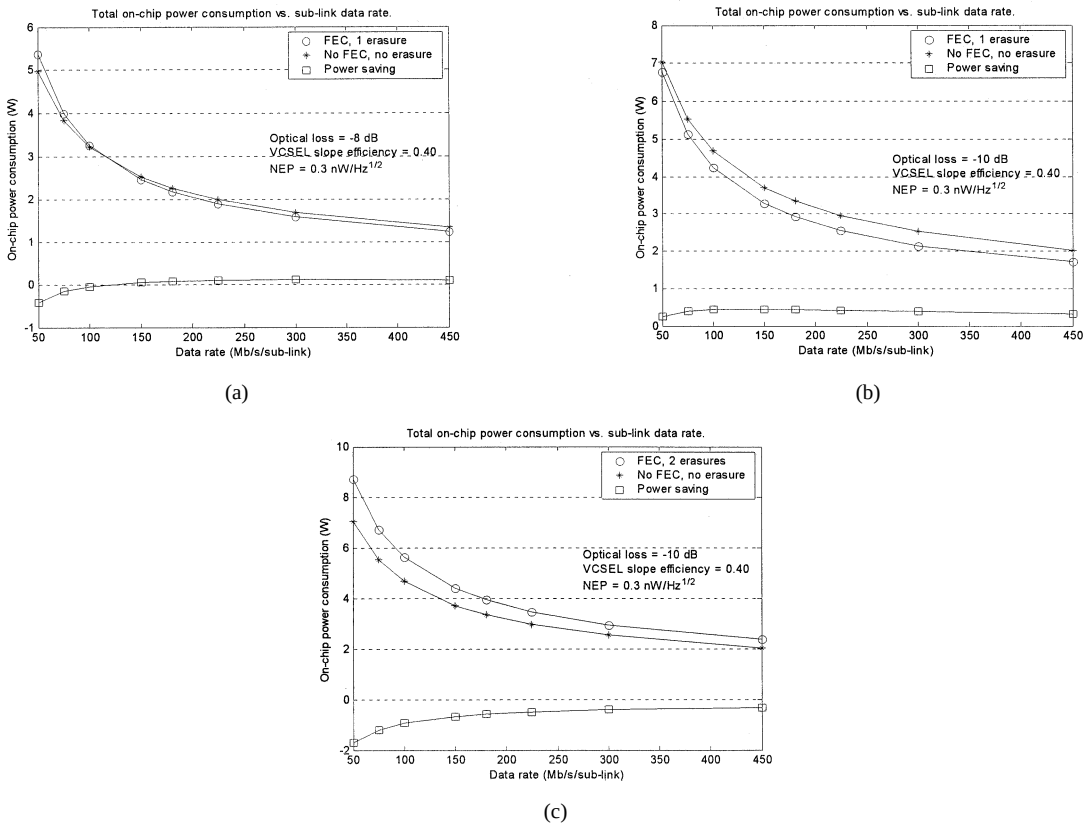


Fig. 6. (a) and (b) On-chip power consumption for two 2-D-ODLs. One has no FEC and no erasure, and the other one has FEC and one erasure. (a) Is $-8$ dB of optical losses and (b) is $-10$ dB of optical losses. (c) The second 2-D-ODL has FEC and two erasures. The NEP and the VCSEL slope efficiency were assumed to be 0.3 nW/Hz$^{1/2}$ and 0.4 mW/mA, respectively.

the Golay decoder offers a better aggregate error-correction capability (parameter $T$ in Table I) than the RS decoder if the erasures are spread out randomly across the array. If, on the other hand, the erasures are found to be clustered, then the RS decoder has the best aggregate error-correction capability. Hence, the required aggregate data rate, the available area on the ASIC, and the distribution of the errors across the array will ultimately determine which FEC code is better suited for 2-D-ODLs. In general, if a low-latency and area-efficient parallel decoder exists for a given code, then this work can help predict the impacts of using on-chip FEC for this code.

In summary, we have developed a model that allows for quantitative comparison of the overhead required in implementing Golay code-based FEC in 2-D-ODLs. Using this system model, we have demonstrated that on-chip FEC will 1) reduce the required VCSEL launched power to achieve a given BER; 2) keep the BER below the target BER in the presence of erasures; 3) reduce the on-chip power consumption; and 4) relax the optical throughput requirement. We have found at certain data rates and optical throughput conditions that implementing on-chip FEC will cause a power penalty but will permit operation of a 2-D-ODL that would otherwise be inoperative due to erasures and/or optical losses. These results will be useful in designing optically interconnected electronics based on 2-D-ODLs by allowing for the system electronics to provide reliability and robustness and subsequently relaxing optical-system requirements.

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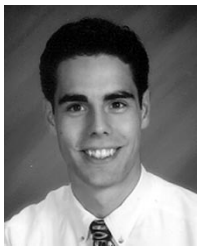

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