512-channel vertical-cavity surface-emitting laser based free-space optical link

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A vertical-cavity surface-emitting laser based bidirectional free-space optical interconnect has been implemented to interconnect two printed circuit boards. A total of 512 clustered channels with a density of 2844 channels/cm² are transmitted over a distance of 83 mm. The optical interconnect is a combination of refractive microlenses and diffractive minilens relays. © 2002 Optical Society of America OCIS codes: 200.2610, 200.4650, 220.4830, 200.4880, 250.7260, 350.3950.

1. Introduction

Parallel optical interconnects have great potential for use as high bandwidth interconnects over short distances, such as at the board-to-board and shelf-toshelf levels.¹ Parallel optical interconnects offer compact, high capacity interconnections with low power requirements. Recent developments in the integration of large vertical cavity surface emitting laser (VCSEL) arrays on complementary metal-oxide semicondutor(s) CMOS(s) increase the potential of parallel optical interconnects.^{2–5}

A variety of approaches have been taken to implement such optical interconnects. Unidimensional parallel optical data links, linear VCSEL arrays, and fiber ribbons have demonstrated high performances in recent years.^{6–10} More recently, fiber image guides showed the possibility of propagating twodimensional (2D) channel arrays.^{11–13} These guided mediums offer flexible connections that have the advantage of requiring alignment only at the ends of the link. Free-space optical interconnects (FSOIs) have greater alignment challenges, but they are potentially more suitable for short distance optical connections on the order of centimeters. Over such short distances, FSOIs can image very large 2D channel

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arrays through a small optical window resulting in a larger channel density. In addition, microoptic elements used in free-space systems can be made of plastic^{14–17} and be mass produced by injection molding or embossing techniques. This can considerably reduce the cost of the links.

A possible use for the FSOIs is to interconnect printed circuit boards (PCBs) fixed in a rack as shown in Fig. 1(a) as a replacement for an electrical backplane. The dense optical interconnects will offer more bandwidth than a standard electrical bus. In this paper, we present the design, assembly, and test of a bidirectional VCSEL-based free-space optical link. The link is to be used to interconnect two printed circuit boards lying on the same plane as shown in Fig. 1(b). This configuration differs from the bookshelf arrangement of the optical backplane illustrated in Figure 1(a), but was chosen to simplify the assembly and characterization of the system. Furthermore, it represents a precursor to the rackbased system. The center-to-center separation of the two chips was specified as 83 mm, which is equivalent to the optical throw that would be required for a 1 in. board separation in the bookshelf configuration. Because the two printed circuit boards are lying on the same plane, two prisms were required at each end of the optical link to redirect the beams onto the detectors. The VLSI optoelectronic (OE) chips were hybrid Si-GaAs devices, with 256 VCSELs and 256 photodiodes. The VCSELs were proton implanted and were designed to operate at 850 nm with a threshold current of \sim 4.5 mA and slope efficiencies of 0.25 mW/mA. The devices were designed to be backside emitting and were flip-chip bonded to CMOS driver circuits. The GaAs substrate was later removed after flip-chip bonding to minimize

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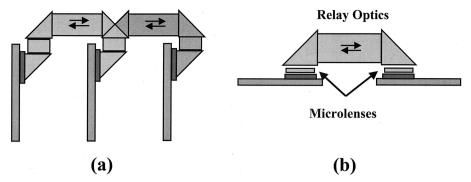


Fig. 1. (a) Illustration of a free-space optical link in a rack configuration, (b) implemented configuration.

light absorption. The photodiodes were p-i-n structures designed to operate with a responsivity of 0.5 $A/W.^4$ An optical interconnection between these two chips had already been demonstrated with a macrolens system.² However, this optical system was bulky and did not represent a practical implementation.

Throughout this paper, the term optical channel refers to the route that propagates a single VCSEL onto its corresponding detector. A total of 512 optical channels were therefore required to bidirectionally interconnect the two chips. The optical link consists of both collimating/focusing optics and relay optics.

The format of this paper is as follows: Section 2 describes the optical design of the different modules that compose the parallel free-space interconnect and the results of a misalignment analysis. In Section 3, the assembly procedure, the alignment techniques used as well as a description of the opto-mechanical components are discussed. Section 4 presents the characterization results of the assembled optical link. In Section 5, the functionality and the bidirectionality of the system is demonstrated by transferring digital data through the link. Finally, Section 6 concludes the paper with a discussion of possible improvements to the link.

2. Optical Design

There are three relay configurations that are commonly used in FSOIs.^{1,18} The simplest of these is the macrolens configuration in which a pair of telecentric lenses images the entire device array. Although a long optical throw can be achieved with this configuration, it requires fast lenses with large fields of vision and very low aberrations. Even if collimating the VCSELs by use of microlenses would enable the employment of slower lenses,^{17,19} this design does not scale well with the field of view. At the other extreme, a microchannel arrangement would include pairs of microlenses for each individual channel.^{14,20} This configuration scales well as the device array increases in size but the throw distance is limited due to diffraction.¹ Multiple relay stages would therefore be required, which would complicate the assembly. A clustered or minichannel system is intermediate between these two extremes and has already been implemented in some systems.^{21,22} In this approach the object and image planes are divided into clusters of elements and telecentric pairs of minilens arrays are used to image between them.

A clustered minichannel configuration was chosen for the interconnection. A microlens array was used to collimate the fast beams emitted from the VCSELs to obtain high f/number beams in the telecentric link. Slow beams enabled a larger throw distance of the telecentric relays and provided a better balance between lateral and tilt misalignment tolerances.²³ The optical system was therefore divided into two modules (Fig. 2). The first, referred to as the chip module, is formed by the CMOS chip together with the collimating microlens array. The second, the re-

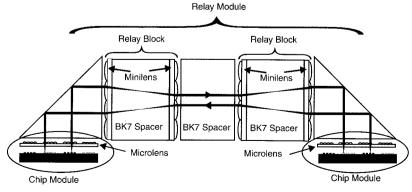


Fig. 2. Schematic drawings of the free-space optical link.

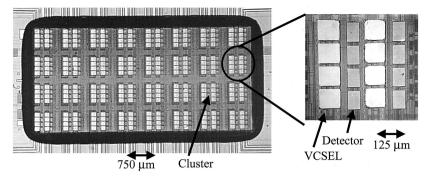


Fig. 3. Photograph of the chip showing the clustered layout.

lay module, was composed of the telecentric minilens pairs. Both modules can be designed and assembled separately. This enabled each block to be individually characterized and results in better misalignment tolerances of the components.^{21,24}

The design of the optical link was guided by the following requirements. First, the pitch between the active elements on the VLSI-OE chips was fixed to $125 \mu m$. The number of VCSELs and detectors was specified to be 512 devices and the center-tocenter separation of the chips was 83 mm. The only flexibility in the layout was to group the active devices within clusters by discarding one or more rows and columns on the required 125-µm grid. It follows that clustering the VCSELs/detectors increased the chip size, creating two conflicting requirements.²⁵ The separation of the clusters should be minimized to maximize the fraction of the GaAs die used. However, to avoid beam clipping in the relays, the size of the active device array in the center of each cluster should be small compared to the diameter of the imaging minilenses. Finally, the bidirectional nature of the system requires a symmetric optical link.

Within these requirements, the design parameters were optimized through an evaluation of the maximum throughput as well as a misalignment analysis. A ray-tracing algorithm was used for these simulations. Although as has been shown²⁶ that this leads to inaccuracies in the estimation of misalignment tolerance when compared to a wave-propagation model, the additional computation time did not justify the improved accuracy in this case.

Å Monte Carlo-radiometric analysis was used to estimate the throughout of the system for different parameters and misalignments. Rays were launched at random with a spatial probability density function defined by the mode field diameter of the VCSELs and with an angular probability density-function defined by their divergence angle. The multimode VC-SELs used in the system had a mode field diameter of 6 μ m and a full divergence angle of 20°. A total of 5000 rays were propagated through the system for each simulation. At the other end, the detector was represented by a 50 μ m × 50 μ m surface, which was equivalent to the detector size on the real CMOS chip. The throughput was calculated as the fraction of all

rays incident on the 50- μ m detector aperture. In all the simulations, the VCSEL located in a corner of a cluster was modeled. This beam was the closest to the edges of the minilenses and therefore suffered the most from clipping and misalignment of components in the system.

The diameter and focal length of the collimating microlenses were determined by the VCSEL pitch $(125 \ \mu m)$ and the beam divergence angle (20°) . To avoid clipping the beams, the focal length was set to 250 μ m. The resulting refractive f/2 microlenses were circular with a pitch of $125 \ \mu m$. Plano-convex fast lenses, such as these microlenses are more subject to aberrations. Simulations showed that if the convex side of the collimating lenses was facing the VCSELs, the spherical aberrations introduced by the lenses could limit the maximum throughput of the optical link to 85%. This value of throughput was unacceptable given that the lost power would also contribute to crosstalk. For that reason, the beams emitted from the VCSEL needed to be first refracted by the planar surface of the microlens array substrate. A 300-µm thick fused-silica substrate was therefore selected to be able to position the chip at the focal plane of the microlens array. This left a distance of 44 µm between the VCSELs and the substrate. The use of a thin substrate introduced complex fabrication and packaging problems. The manipulation of such substrates during the fabrication process as well as the precise alignment required at a distance of 44 μ m from the VCSELs/detectors were delicate tasks. However, being so close to the chips, the thin substrate could also be used to seal the OE package if a hermetic seal was required.

The design of the telecentric relay modules is determined by a trade-off between the number of channels per cluster and the cluster size. To maximize the fraction of the GaAs used, the chosen values were clusters of 4×4 active devices, separated by a centerto-center distance of 750-µm. The 512 OE devices were therefore grouped in 4×8 clusters within a chip area of 5.625 mm \times 2.625 mm and were propagated in an optical window of 6 mm \times 3 mm. The resulting channel density was 2844 channels/cm² and this design utilized 54.2% of the OE devices growth on the GaAs wafer (assuming a 125-µm grid). The layout

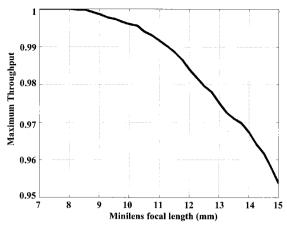


Fig. 4. Maximum throughput as a function of the minilens focal length for a 750-µm cluster pitch.

of the devices is shown in Fig. 3. The focal length of the relay minilenses needed to be sufficiently large to propagate the VCSEL beams over the required 83 mm. Via the ray-tracing simulations, the throughput of a corner channel in each cluster was calculated as a function of the relay minilens focal length (while maintaining a telecentric configuration). The graph in Fig. 4 shows the results of this throughput simulation for the 750-µm cluster. It can be seen that for a fixed cluster size, the throughput of the optical link drops rapidly as the focal length of the relay module is increased. This is due to vignetting at the first minilens. Because the power lost appears as crosstalk to adjacent clusters, it was concluded that the maximum usable focal length was 8.5 mm. Therefore, at least two consecutive relay modules were needed to provide the required optical throw distance, as shown in Fig. 2.

The separation of the two minilens arrays in each relay block was controlled through the use of precisely polished BK7 glass spacers. These glass spacers also increased the physical length of the relay. This design choice resulted in modules that were more robust and that could be assembled separately. The BK7 spacers allowed the use of two consecutive relay blocks with a focal length of 8.5 mm to interconnect the VLSI-OE chips over the 83 mm that separates them. The f/8 minilens arrays were fabricated as diffractive elements by use of a gravscale mask process on a 1-mm thick fused-silica substrate. The 256 etch depths available from the fabrication process allowed high and uniform diffraction efficiency. While the lens array dimension was 6 mm \times 3 mm, their substrates were diced to 20 mm \times 6 mm to leave space for alignment features and assembly components as discussed in Section 3.

The two 45° prisms were also made of BK7 and were fixed at one end of the relay blocks. The prisms were larger than the relay modules by 5 mm to enable a passive alignment of the link to the chip module (see Section 3).

The characteristics of the microlens and minilens arrays are summarized in Table 1.

Table 1. Lens Array Specifications

| Specifications | Microlens, | Minilens, diffractive |
|---|---|--|
| lens type | refractive | (256-level) |
| Focal length Array size Dimension Substrate thickness | $250 \ \mu m$ $8 \times 4 \ clusters \ of 4 \times 4$ $125 \ \mu m \ diameter$ $300 \ \mu m$ | 8.5 mm 8×4 $750 \ \mu\text{m} \times 750 \ \mu\text{m}$ $1 \ \text{mm}$ |

Results of Misalignment Tolerance Analysis.

The tolerance to misalignment of the optical components was calculated to determine the assembly and integration precision that would be required. This was performed by moving a single element or a group of elements together while keeping the rest of the system undisturbed and calculating the throughput via ray tracing. The misalignment tolerances are summarized in Table 2. The limits for an acceptable tolerance have been set to 95% of the maximum throughput for the whole system. The choice of a 95% throughput value is somewhat arbitrary but since many of the misalignment curves are quite steep, it provides a reasonable insight into the tolerance of the system. In the case where the misalignment curves were not symmetric around the origin, symmetric tolerances were taken with a value equal to the smallest misalignment bound. This assumption is valid because the simulations of the opposite corner channel gave the same results, but mirrored around the origin.

It should be noted that the throughput simulations do not include losses due to diffraction efficiencies, Fresnel reflections, and absorption. Taking this into account resulted in an estimated throughput of between 50% and 65%.

Simulation results show that grouping the optical elements within modules gives better misalignment tolerances.^{21,24} For example, the VCSEL or the microlens alone have a lateral misalignment tolerance of \pm 2.5 µm. Once they are attached to each other, the resulting chip module has a tolerance of \pm 25 µm. The alignment of the microlenses to the VCSELs is the most critical task. However, this tolerance was achievable through the use of active alignment. The quoted misalignment tolerance of \pm 90 µm between the two relays and the chip modules represents the required alignment of the relay block to the chip modules if the two chips were in perfect mutual align-

Table 2. Misalignment Tolerances

| Misaligned Elements | >95% Tolerance |
|--|---|
| VCSEL (in x) | $\pm 2.5 \mu m$ |
| First microlens (in x) First VCSEL-microlens (in x) | ${\pm}~2.5~{ m \mu m}$ ${\pm}~25~{ m \mu m}$ |
| First relay (in x) Two relays (in x) | $\pm 12.5~\mu{ m m}$ $\pm 90~\mu{ m m}$ |
| VCSEL (in z) | $\pm 15 \ \mu m$ |
| First VCSEL-microlens (in z) | \pm 2.0 mm |

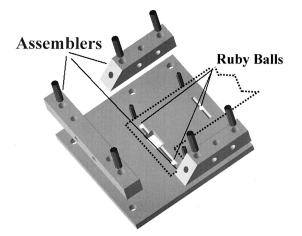


Fig. 5. Schematic of the microlens holder with the removable assemblers. The dotted line represents the contour of the optical link.

ment with each other. In practice, this is unlikely to occur and so the real tolerance is $\pm 25 \ \mu m$. The minilens arrays were aligned together by use of an interferometric technique.²⁷ In this case, the technique enabled an alignment better than $9 \mu m$, which is within the required tolerances. The two relays were assembled together by using the same alignment method. The block formed by the two relay modules has a larger misalignment tolerance and can be passively aligned to the chip module. Because a rotational misalignment translates into a displacement in x and y, its tolerance was therefore treated in the lateral alignment study. The tilts $(\theta x, \theta y)$ misalignment tolerances were assumed to be of the same order as a similar FSOI²¹ which had a worst-case tolerance of $\pm 0.05^{\circ}$. This precision can be achieved by using the retroreflected beam method.²⁸

3. System assembly

A total of 11 optical elements needed to be precisely aligned and glued together in the system. Custom opto-mechanical mounts were designed to properly align the optical elements as well as to hold the resulting link. An example is the mount illustrated in Fig. 5, which was designed to provide the interface between the modules. This component, referred to as the microlens holder, acted as the mechanical reference between the chip and the relay module. On the top of the microlens holder, three ruby balls defined a plane on which the relay module was seated. This platform minimized the tilts between the two modules. The lateral positioning of the link on the microlens holder was determined by three dowel pins. This alignment method required the BK7 spacers used in the relay block to be well polished on their sides. It also required the minilens substrates to be aligned to the edges of the glass spacer assembly of the relay block and finally the prisms to be aligned to the same edges. To assist in the assembly of the system, removable mounts ("assemblers") were incorporated into the microlens holder.

The microlens substrate was suspended below the holder on a precisely machined standoff mount. This standoff ensured that the holder did not come into contact with the wire bonds while the microlens substrate (Fig. 6) was being was being positioned. The height of the standoff determined the distance between the microlenses and the minilenses.

A. Chip Module Assembly

The first step in the chip module assembly was to attach the microlens substrate to the standoff beneath the microlens holder. Lithographically defined metal marks were deposited on the microlens substrate during the fabrication process. These markers were used to position the substrate relative to the microlens holder. The resulting package was attached to the chip carrier after aligning the microlenses to the VCSELs/detectors. The positioning of the microlens was a delicate task given the tight misalignment tolerances. For this alignment, the microlens holder was mounted on a six degrees-offreedom micropositioning stage and was brought close to the OE chip. First, the tilt alignment was performed by illuminating the substrate with a large monochromatic plane wave and by minimizing the number of interference fringes produced by the partial reflections from the microlens substrate and the chip surface. To maximize the fringe contrast, a HeNe laser was used for its long coherence length and also because its wavelength differs from the one for which the antireflection coating of the substrate was designed for. A worst-case misalignment of 0.02° could be achieved with this method.

Next, the substrate was brought to the required distance from the VCSELs. A 44- μ m high epoxy wall surrounding the OE devices ensured the required VCSELs-microlens separation.

The lateral alignment was done actively by turning on the VCSELs. The beams collimated by the mi-

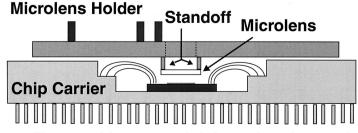


Fig. 6. Illustration of the steps onto which the microlens substrate is glued.

crolenses were projected on a screen on which they could be observed with a CCD camera. The lateral and roll alignments were realized by optimizing the intensity of the spot observed as well as their uniformity. The sensitivity enabled the microlens array to be aligned to the OE devices within the required \pm 2.5 µm precision calculated in Section 2. Once the alignment was achieved, the microlens holder was glued to the chip carrier to form the chip module. Two types of glue were used: first a low-shrinkage UV glue and furthermore an epoxy. The epoxy was used to bridge the 300-µm gap between the two components, while the UV glue was used to avoid a drifting of the aligned components while the epoxy was setting.

B. Assembly of the Relay Modules

The passive-alignment technique of the relay module to the microlens holder required the minilens substrate to be smaller than the glass spacers of the relay blocks and precisely positioned relative to their edges.

Once the first minilens substrate was attached to the glass spacer, the second minilens array of the relay block was aligned laterally to the first with four interferometric lenses.²⁷ The interferometricalignment technique, in which low-efficiency diffractive lenses produce fringes, has already demonstrated successful results.²¹ The number of fringes determines the misalignment of the components according to the following equation:

$$\Delta x = f_{\rm L} * \tan\left[\sin^{-1}\left(\frac{N\lambda}{D_{\rm L}}\right)\right] \tag{1}$$

where Δx corresponds to the misalignment, $f_{\rm L}$ and $D_{\rm L}$ to the focal length and dimension of the interferometric lenses, N is the number of fringes, and λ the wavelength used. In the design, the interferometric lenses were 1.2 mm by 1.2 mm and had a focal length of 8.5 mm. Designed to be used with a HeNe laser ($\lambda = 632.8$ nm), a lateral alignment better than ± 4.5 µm could be achieved as well as a rotational alignment around the center of the array of better than 0.05°. The angular alignment was determined by the parallelism of the end faces of the BK7 spacers (better than 0.05°).

The prisms needed to be aligned with the minilens array, because their edges were also used to reference the relay module to the microlens holder. However, because it was not possible to put alignment features on the prisms, a passive-alignment technique was therefore required. An L-shaped module formed by three parallel rods was used to assemble the prisms to the relay blocks. Ceramic spacers (0.8-mm thick) were used to fix the prisms and to ensure an air gap between them and the diffractive minilenses.

The two relay blocks were attached to each other in an L-shaped holder to form the relay module. The lateral alignment of the relay was performed by using a second set of interferometric lenses. The longitudinal separation of the two modules was fixed by a

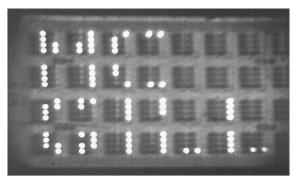


Fig. 7. Beams being focused by the last microlenses (over illuminated). Alternating VCSEL on and off.

third BK7 glass block. Once attached to the L-shaped holder, the optical-link package was robust and could be aligned to the chip modules.

The final alignment of the chip modules to the relay module was challenging. The alignment could not be monitored, and its precision could only be confirmed by sending data through the link. However, the large misalignment tolerances of the modules allowed a passive assembly of the chip and relay modules. Figure 7 shows the beam after the last microlens array.

4. Characterization Results

After the first chip module had been attached to the relay module, characterization measurements were performed. A microlens holder with only the microlens substrate was temporarily fixed to the second end of the optical link. This allowed measurements on the beams at the second chip plane. The spot size, power uniformity across the clusters, efficiency, and optical crosstalk were calculated.

A. Beam Characteristics

Spot size and beam uniformity were measured with a 2D power scan. This was achieved through the use of an optical power meter with a pinhole aperture that was scanned across the beam array at the chip plane with a motorized micro-positioning stage. The results of this scan are shown in Fig. 8(a). The diameter of the pinhole was 4 μ m and the scan steps were 2 μ m.

Figure 8(b) is a slice of the 2D data of Fig. 8(a). It shows that the spot profile is close to a Gaussian profile. The measured spot size (ω) was 12.55 μ m on average and the variation between the beams is small (12.30 μ m–12.81 μ m). The spot size is therefore smaller than the desired maximum size of 16.6 μ m. The power uniformity of the beams within a cluster was, however, worse than expected. The standard deviation of the beam power within the cluster was on average 35% of the mean. From Fig. 8(a) it can be seen that the beams closer to the edges of the clusters contain less power than the central ones. This non-uniformity is assumed to be due to beam clipping in the relays. However, there was very little difference in performance from cluster to cluster, demonstrat-

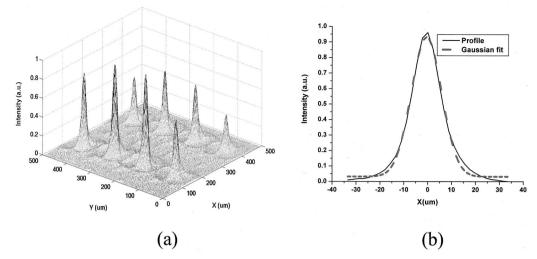


Fig. 8. Results of the power measurements of the beam at the detector plane, (a) 2D map of a cluster, (b) profile of a beam.

ing the scalability of the link. The standard deviation between clusters was 6.9% of the mean.

B. Optical Efficiency

Two measures of power transfer were calculated for the optical interconnect. The first, the throughput, provides an estimate of the losses of the link. For this measurement, all the VCSELs were turned on, and the power was measured after the final microlens. This reading gives the total power that is transmitted to the second chip and includes the power that would fall between the photodetectors. Taking the ratio of this power reading with the total power emitted by the VCSELs (measured before the assembly) gives the amount of power lost during the propagation into the optical link. This throughput was found to be 31%, which is lower than the 50-65%predicted. That represents an optical power loss of 5.1 dB. Further measurements showed that at least 21% (1 dB) of the power was leaking from the first prism. Figure 9(a) shows the light leaking from the prism. It can be observed that the intensity of the spot is greater on the left-hand side. This demonstrates that a portion of the beams hit the prism at an angle smaller than the total internal reflection angle as illustrated in Fig. 9(b). It is thought that the beams from the multimode VCSELs were not perfectly collimated by the microlenses because of both the multimode nature of the beams as well as the longitudinal misalignment between the VCSELs and the microlenses.

The second power transfer measurement can be referred to as the efficiency of the link: It is based on the power falling onto the detector. It was measured by attaching a pinhole to the power meter detector. The diameter of the pinhole was chosen to match the side length of the hybridized detectors. First of all, the ratio of the power that would fall on the detector over the total transmitted power of the corresponding VCSEL was calculated for each individual channel. The real efficiency is the combination of this ratio and the link throughput previously

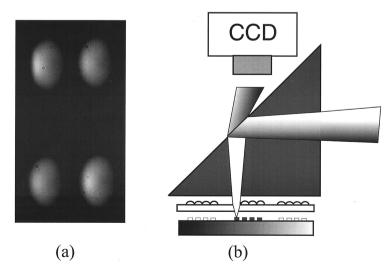


Fig. 9. Light leaking from the prisms (a) obtained from the setup illustrated in (b).

Table 3. Results of the Optical Link

| Characterization | Minimum | Maximum | Average |
|---------------------|-----------|--------------------|--------------------|
| Throughput | _ | _ | 31% |
| Efficiency from the | 25.3% | 39.0% | 34.3% |
| second microlenses | | | |
| Total efficiency | 6.6% | 11.7% | 9.0% |
| Crosstalk | -10.6 dB | $-8.0~\mathrm{dB}$ | $-9.6~\mathrm{dB}$ |
| | | | |

calculated. It represents the ratio of the power that would hit the detector on the chip over the power emitted by the corresponding VCSEL. The results are given in Table 3. The results showed that on an average, 34.3% of the light that was propagated through the link hit the proper detector. The real efficiency is therefore the product of this value with the link throughput (31%) and is equal to 9%. This is lower than the predicted value of between 50% and 65% due to the excess loss at the prisms. Note that this loss could be avoided by coating the prisms.

C. Crosstalk

The optical crosstalk was also measured before the final attachment of the second chip. The method used is similar to the one presented in the previous Subsection 4B for the efficiency measurements. The same pinhole, equivalent to the size of the hybridized detectors, was positioned in front of the power meter detector. All the VCSELs were turned on and the pinhole was aligned on a channel at the second chip plane. The power was recorded and the corresponding VCSEL was turned off. The new reading gave the power from the 250 remaining VCSELs (5 were defective) that was routed to the channel under test. An average of -9.6 dB crosstalk was measured. This crosstalk calculation is also the worst-case crosstalk as obtained from the contribution of all VC-SELs surrounding the channel.

5. Data Transfer

After the characterization measurements presented in the previous section, the microlens substrate was replaced by the second chip module. The complete system is shown on Fig. 10. The boards used for the data transfer were designed to test the functionality of the chip and were therefore not high-speed boards. The maximum data rate achieved for a single channel was 2 megabits per second. This is lower than the 50 megabits per second recorded with the macro-optical relay (using the same boards and chips).² This reduced speed is attributed to the low power incident on the detector due to the poor efficiency of the link.

The poor uniformity of the beams in the cluster combined with the architecture of the chip, which did not enable individual trimming of each receiver, made it difficult to optimize the detector parameters for all the channels simultaneously. To get multiple channels working within the same cluster, the data rate needed to be further reduced.² At a data rate of 0.5 megabit per second, 4 channels out of the 32 that were commonly controlled were able to simultaneously operate. Furthermore, to demonstrate the bidirectionality of the link, data were transmitted from the two boards simultaneously and were successfully received by their corresponding detectors over two channel pairs at a data rate of up to 0.1 megabit per second.

6. Conclusions

We have successfully implemented a bidirectional 512channel free-space optical interconnect between two CMOS chips containing hybridly attached VCSELs and detectors. To achieve a channel density of 2844 channels/cm² and an optical throw of 83 mm, modeling indicated that neither a macrooptical nor a minichannel system would be practical. Instead, a clustered minichannel approach was taken. In this configuration, the optical channels were grouped within 4×8 clusters of 4×4 channels. The pitch of $125 \ \mu m$ between the active devices was determined by the VCSEL supplier. The 750-µm cluster size is a trade-off value chosen between the minimization of the area of GaAs used and the maximization of the misalignment tolerances of the components of the link.

Simulations demonstrated that the spherical aberrations of the microlenses that collimate the VCSELs'

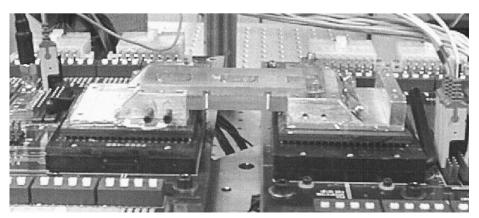


Fig. 10. Photograph of the assembled system.

beams limited the performance of the system and needed to be minimized by having the flat surface of the microlens substrate facing the VCSELs. This constraint added complexity to the link assembly because the microlenses were fabricated on a thin substrate that needed to be aligned at 44 μ m from the VCSELs. The simulation also showed that grouping the optical elements into modules results in a better misalignment tolerance. The chip and relay modules were assembled and characterized individually.

Results showed an optical efficiency of 9% and an optical crosstalk of -9.6 dB. One of the main contributions to excess loss was found to be leakage from the prisms (approximately 1 dB each) as well as the beam clipping within the relays. This can be attributed to a poor collimation of the VCSELs beams due to their multimode nature and possibly a longitudinal misalignment of the microlenses in the chip module. These losses could be reduced by coating the reflective surface of the prisms and by better modeling of the multimode nature of the VCSELs. In spite of the poor efficiency and crosstalk, we demonstrated unidirectional and bidirectional communication between boards.

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