Six-degrees-of-freedom alignment of two-dimensional array components by use of off-axis linear Fresnel zone plates

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A novel six-degrees-of-freedom (six-DOFs) alignment technique for assembling two-dimensional array components is presented. The technique uses off-axis linear Fresnel zone plates on one component that are combined with alignment targets on the other. The technique is compact and sensitive to all six DOFs; it was used to package an array of microlenses with a 32 × 32 array of GaAs multiple-quantum-well modulators flip-chip bonded to a 9 mm × 9 mm complementary-metal-oxide-semiconductor chip. By use of interference fringes to control the tilt misalignment, the worst-case misalignment of the microlenses relative to the chip is calculated to be as follows: lateral = 3.0 μm, rotational = 0.023°, longitudinal = 13 μm, and tilt = 0.022°. We also propose alternative implementations of the technique, including one that uses on-chip photodetectors to automate this six-DOF alignment technique.

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1. Introduction

Two-dimensional free-space optical interconnects (2D-FSOIs) can provide high-density and high-speed communications between VLSI chips in computing and switching systems.[1,2] Research in this field has experienced significant progress in recent years, primarily owing to the advances made in the areas of optoelectronic VLSI (OE-VLSI) and micro-optics technologies.[3–7] Despite this, the construction of highly parallel 2D-FSOI systems remains a difficult task largely owing to the lack of cost-effective assembly techniques capable of achieving and maintaining alignment, particularly in harsh industrial environments. This alignment problem originates from the fact that current systems are constructed with discrete components that must be aligned in three spatial and three angular coordinates to within tolerances that often exceed standard mechanical machining capabilities. To alleviate the problem, system designers usually integrate components together to form rigid modules; this decreases the total number of degrees of freedom and reduces assembly complexity.

At the end points of the interconnect, where the OE-VLSI chip interfaces with the optical system, a modular approach is usually a necessity. This is because light sources and sinks, whether they are OE devices or fiber cores, are small in size and thus require low *f*-number beams. In contrast, modules that are designed to be tolerant to misalignment use high *f*-number input–output beams; this is because "slow" beams provide a better balance between lateral and tilt misalignment tolerances.[8] These conflicting requirements are usually resolved by integrating microlenses with the device arrays. In doing so, the microlenses are used to transform the low *f*-number beams required by the end devices into high *f*-number input–output beams, the size of the beam ultimately determining the relative distribution between lateral and tilt misalignment tolerances.[9] It follows that proper optical designs can significantly relax the misalignment tolerances of modules. Research in this area will ultimately lead to systems that are passively assembled with snap-

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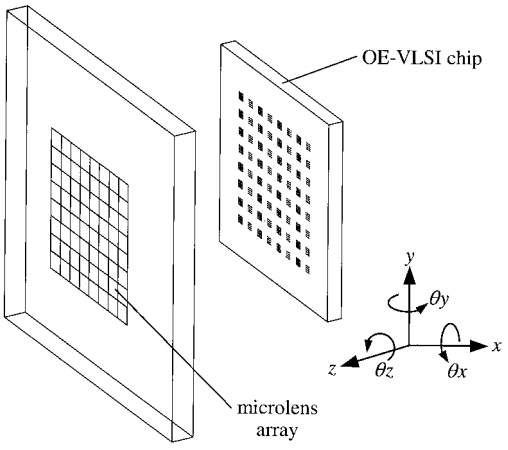

Fig. 1. Six-degrees-of-freedom (x, y, z, θx, θy, θz) alignment of an 8×8 array of microlens to an OE-VLSI chip.

together modules,[10] a prerequisite for the commercial deployment of 2D-FSOI technologies. The realization of passively aligned systems relies on the prior development of cost-effective alignment techniques for assembling 2D array components into modules.

This paper addresses the above issues by presenting a novel optical technique for the alignment of 2D array components in all six degrees of freedom (DOFs) (x, y, z, θx, θy, θz). The technique was developed to perform the six-DOF alignment of an 8×8 array of microlenses to a 32×32 array of GaAs multiple-quantum-well (MQW) modulators flip-chip bonded to a 9 mm $\times$ 9 mm complementary-metal-oxide-semiconductor (CMOS) chip,[11] as shown in Fig. 1. This OE-VLSI chip supported 1024 free-space optical interconnections between adjacent printed circuit boards in a photonic backplane demonstrator system.[12] The alignment technique uses on-chip linear Fresnel zone plates (FZPs) to generate optical alignment features in the plane of the microlens array. The FZPs are designed as off-axis reflective lenses; they are implemented by use of the top-level metal layer of a standard CMOS process. The alignment technique is compact and accurate; it differentiates itself from previous optical methods in that it is sensitive to all six DOFs and is amenable to automated assembly.

The paper is organized as follows. Section 2 is a review of previously published alignment techniques, both active and passive, used for assembling 2D array components. Section 3 describes the operation of the off-axis alignment technique. We also derive general equations to calculate the worst-case misalignment for each DOF, taking into account the various sources of errors. Section 4 presents the experimental setup used to test the technique, including practical considerations that affect the alignment accuracy. In Section 5 we calculate the worst-case misalignment errors for the case of the OE-VLSI module described in Ref. 11. In Section 6 we propose alternative embodiments of the technique, including one that uses on-chip photodetectors to automate the six-DOF alignment of the chip. Section 7 concludes the paper.

2. Review of Previous Alignment Techniques

Several techniques for aligning microlenses to 2D device arrays have been proposed in the past. These techniques can be categorized as either active or passive, the difference being that active alignment techniques require the activation of the OE devices, whereas this is not the case for passive alignment.[13] The most common active technique consists of operating an array of emitters above threshold and bringing the microlens array into alignment while observing the far-field diffraction patterns of the laser beams with a CCD camera.[14,15] Another active method uses laser feedback effects due to reflections from the microlenses.[16] Drawbacks to active techniques are that they are time consuming, labor intensive, expensive, and not amenable to high-volume production.

For this reason, current research has focused on the development of passive alignment techniques that are further divided into two categories: mechanical and optical methods. The most common mechanical method relies on the use of reflowed solder self-alignment to pull parts into position with an accuracy typically better than 2 μm.[17,18] Other mechanical methods include the selective etching of silicon material to form grooves and hollows,[19,20] the fabrication of microconnecting plugs and sockets made with thick photoresist,[21] and the use of deep proton lithography to fabricate mechanical alignment structures directly into poly(methyl methacrylate) (PMMA) components.[22] Mechanical methods are quite promising because, beyond reducing cost, they provide an avenue for wafer-scale integration. However, they are generally limited to cases in which the alignment planes are close together, and thus they cannot be used in situations in which components are separated by many millimeters. This limitation is also inherent to optical methods designed for performing mask-to-wafer alignment in standard microlithographic techniques. Examples include techniques employing dual-side lithography for the monolithic integration of microlenses on the GaAs substrate[23] and the use of moiré fringes.[24]

In situations in which array components are separated by many millimeters, other optical techniques must be employed. One simple approach consists of focusing an alignment microscope back and forth between the two alignment planes and using fiducial markers on both components to perform the alignment.[25] This technique requires high-precision and linear micropositioning equipment because the alignment accuracy relies on the microscope moving along a line exactly perpendicular to the alignment planes. The method is also tedious and cannot be readily automated. The technique is significantly improved by introducing a beam-splitting element halfway between the alignment planes, allowing both planes to be imaged simultaneously with a static microscope. In one implementation of this approach, the compo-

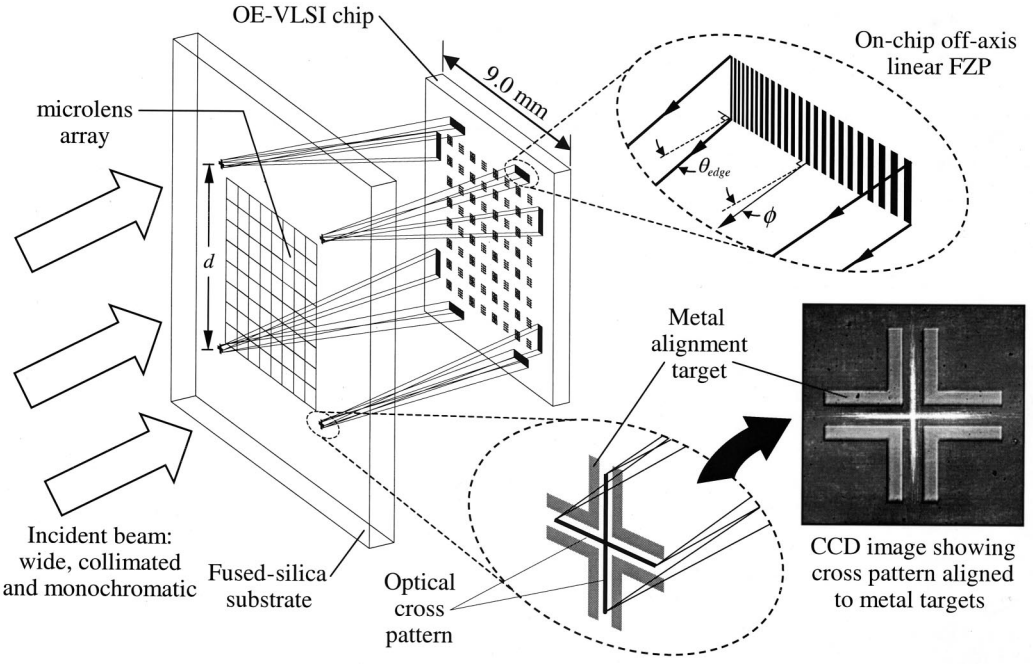

Fig. 2. Description of the six-DOF off-axis alignment technique.

nents are moved away from each other, leaving enough space for a beam-splitter assembly to be placed halfway between the two.[26,27] Once both images are registered, the beam-splitter assembly is removed, and the components are carefully brought in contact. Although this technique avoids the problem of having to focus a microscope back and forth between the alignment planes, it requires high-quality micropositioners and cannot detect misalignment errors that might occur during the last steps of the assembly process when both components are mated and fixed together. This difficulty can be resolved by permanently inserting a partially reflecting flat substrate halfway between the components.[28] Although this approach does not have the drawbacks of the previous method, it does require an additional component and relies on the precise control of the substrate thickness.

An alternative strategy relies on the use of dedicated FZPs fabricated directly on the array components. One technique uses identical circular FZPs on both components, with focal lengths equal to half the component separation.[29] This technique is based on the monitoring of interference fringes generated by overlapping diffraction orders. In the implementation described in Ref. 29, it achieved a lateral sensitivity of ± 3 μm. Another technique uses reflective circular FZPs on one component with alignment targets on the other.[30] In that case, the focal length of the FZPs is equal to the distance between the components. Alignment is obtained by registering the spots generated by the FZPs with the alignment targets. This method was demonstrated with a lateral sensitivity of ± 9 μm.[30] A significant advantage of these two techniques is that they offer real-time alignment monitoring as the components are fixed to one another. This is convenient because it allows for misalignment errors (e.g., walk-off effects during glue curing) to be detected and compensated for. Although these techniques can provide accurate lateral and rotational alignment information, their sensitivity to longitudinal and tilt misalignment is limited by the *f*-number of the Fresnel lenses. For example, the sensitivity to longitudinal misalignment of the techniques demonstrated in Refs. 29 and 30 was of the order of ± 50 μm, making them inappropriate for applications requiring accurate alignment in the longitudinal and tilt DOFs.

The alignment technique presented in this paper is similar to the technique developed in Ref. 30 but with two significant improvements: Linear FZPs consume much less area on the array components, and the off-axis operation of the FZPs offers increased sensitivity in the longitudinal and tilt DOFs.

3. Six-Degrees-of-Freedom-Alignment Technique

A. Description of the Technique

The alignment technique is used to align an 8×8 array of microlenses to an OE-VLSI chip (see Fig. 2). A wide, collimated, and monochromatic beam of uniform irradiance is incident orthogonally to the OE-VLSI chip. The portion of the incident beam falling outside the region occupied by microlenses traverses the fused-silica substrate and illuminates reflective off-axis linear FZPs located on the periphery of the OE-VLSI chip. The FZPs are fabricated by use of the top metal layer of a standard foundry CMOS process, as shown in Fig. 3. The focal length, $f_{\mu\text{lens}}$, is equal to the nominal separation between the microlenses and the chip.

A single linear FZP focuses the incident plane wave

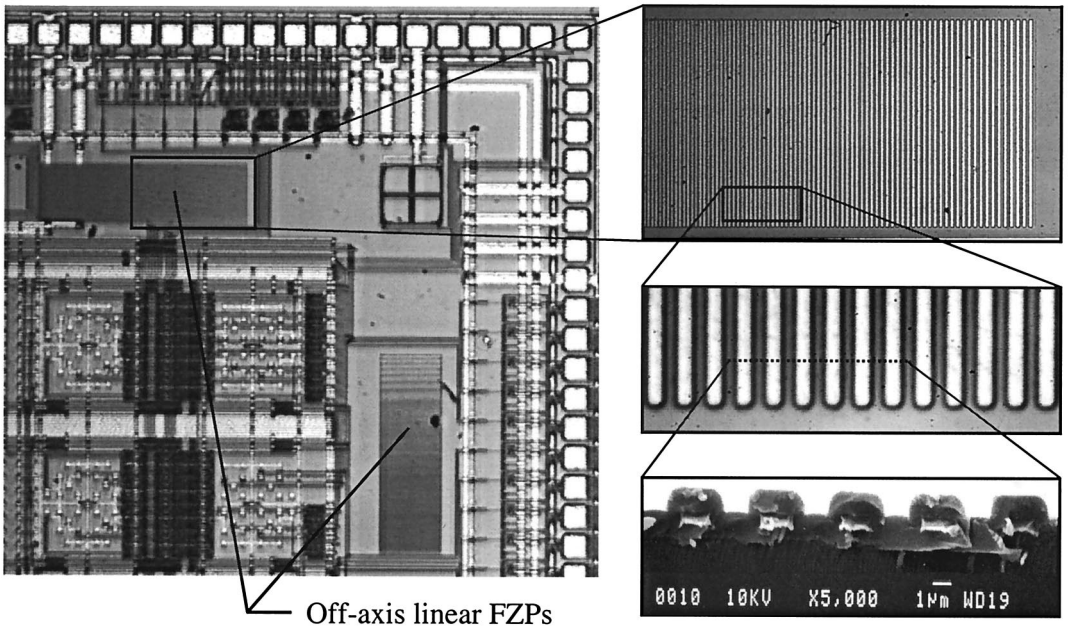

Fig. 3. Photographs of the off-axis FZP fabricated on the CMOS chip.

into a line; a pair of off-axis linear FZPs oriented at 90° to each other is used to generate a cross pattern in the focal plane. Owing to the off-axis operation of the FZPs, the trajectory traversed by the center point of a cross pattern does not follow a line perpendicular to the chip. This means that the center point of the cross pattern shifts laterally as it is imaged at different planes along the optical axis, as shown in Fig. 4.

In the implementation shown in Fig. 2, one FZP pair is placed in every corner of the OE-VLSI chip. Chrome alignment targets (in the form of inverted crosses) are deposited on the microlens-array substrate; these are lithographically defined at the same time as the microlenses. Six-DOF alignment is achieved by positioning the microlens-array substrate such that all chrome targets are registered with the focused cross patterns. Note that only three FZP pairs are necessary; the fourth pair is redundant. This is because the center of three cross patterns in the focal plane uniquely specify the position and orientation (i.e., all six DOFs) of the microlens substrate with respect to the chip.

B. Accuracy of the Technique

In this section we present closed-form expressions for the worst-case misalignment errors for each of the six DOFs. Three sources of error limit the accuracy of the technique. The most important error is due to the incident beam not being perfectly orthogonal to the chip, resulting in the lateral shift of the optical crosses in the microlens-array plane. We define the angle between the incident beam and the chip to be $90° - \beta$. Techniques developed to minimize the value of β are presented in Section 4.

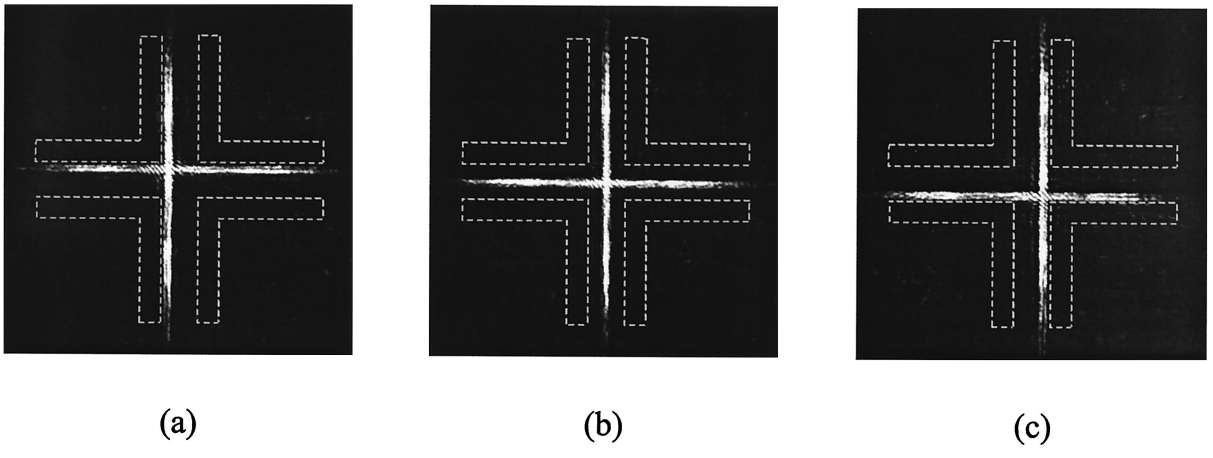

Fig. 4. CCD images showing location of the cross pattern with respect to the fiducial markers (outlined) at three different planes along the optical axis: (a) 100 μm in front of the focal plane, (b) at the focal plane, and (c) 100 μm behind the focal plane.

The second contribution is due to the error in judging when an optical cross is properly centered on its alignment target. This decentration error is defined by a quantity δ, expressed in micrometers. The value of δ depends on various features of the experimental setup, including the magnification of the imaging system, the width of the focal lines making up the cross patterns, the resolution of the CCD camera, the mechanical stability of the positioning equipment, and the use of image-processing software. The value of δ for the setup described in Section 4, which uses a $\times 50$ microscope objective, was estimated to be 2 μm. Finally, the third source of error is due to the finite accuracy of the microlithography processes that are used to fabricate the FZPs on the chip and the alignment targets on the microlens substrate. This last contribution is usually negligible compared with the previous two, and so it is neglected.

Closed-form expressions for the worst-case misalignment errors are derived as follows. The starting point is the assumption of a perfectly aligned microlens array, with an incident collimated beam making an angle $90° - \beta$ with the surface of the chip. For each DOF, the worst-case error is obtained by determination of the maximum misalignment of the microlens substrate in that DOF, which results in optical crosses being decentered by an amount equal to δ. Given the above, the worst-case lateral error $(\Delta x, \Delta y)$ corresponds to the microlens array being laterally misaligned by an amount,

$$\Delta x = \Delta y = \delta + f_{\mu\text{lens}} \tan(\beta). \tag{1}$$

The rotational error $(\Delta\theta z)$ is derived by considering the rotational angle required for optical crosses located at opposite corners of the microlens array to be decentered by an amount δ,

$$\Delta\theta z = \arctan\left(\frac{\sqrt{2}\delta}{d}\right) \cong \frac{\sqrt{2}\delta}{d}, \tag{2}$$

where d corresponds to the distance between adjacent alignment targets. The longitudinal error (Δz) is given by the axial displacement required for optical crosses to be decentered by an amount less or equal to δ,

$$\Delta z = \frac{\delta}{\tan(\phi - \beta)} \cong \frac{\delta}{\tan\phi}, \tag{3}$$

where ϕ is the off-axis angle of the linear FZPs, as depicted in the inset in Fig. 2. The off-axis angle is defined as the angle between a vector normal to the chip plane and the vector connecting the center of an on-chip FZP to the center of its corresponding alignment target, under perfect alignment conditions. In practice, a large value of ϕ is desirable because it reduces Δz; for this reason, it is reasonable to assume that $\phi \gg \beta$.

The tilt misalignment error $(\Delta\theta x, \Delta\theta y)$ corresponds to the tilt required for alignment targets on opposite sides of the microlens substrate to be defocused by an amount Δz in opposite directions, which yields

$$\Delta\theta x = \Delta\theta y = \arctan\left(\frac{\Delta z}{d/2}\right) \cong \frac{2\delta}{d \tan\phi}. \tag{4}$$

As indicated by approximations (3) and (4), the larger the off-axis angle, the more sensitive the technique to longitudinal and tilt misalignments.

C. Design Considerations

The off-axis angle, ϕ, can be increased in two ways: (i) by increasing the diffraction angle on the outside edge of the FZP, θ_{edge}, by adding high-order zones and (ii) by removing low-order zones on the inside of the FZP. The maximum value of θ_{edge} is usually limited by the minimum feature size allowable by the fabrication technology. For the implementation discussed in Section 5, this limitation was dictated by the CMOS design rule for the top metal layer that specifies a minimum metal width and spacing of 2.0 μm. Using the grating equation,[31]

$$\sin(\theta_{\text{edge}}) = \frac{m\lambda}{p}, \tag{5}$$

where m is the diffraction order, λ is wavelength, and p the grating period. Assuming $m = 1$, $\lambda = 0.85$ μm, and $p = 4.0$ μm, this results in a maximum edge diffraction angle of 12.3°.

The removal of low-order zones increases the value of ϕ but reduces the lens aperture; this increases the width of the focal lines forming the cross patterns, resulting in an increase of δ. This leads to the following design compromise. On the one hand, too small a value of ϕ yields a poor sensitivity to longitudinal (z) and tilt $(\theta x, \theta y)$ misalignments. On the other hand, increasing the value of ϕ by removing low-order zones eventually decreases the sensitivity in the lateral (x, y) and rotational (θz) DOFs. Determining the optimum value of ϕ with an analytic approach is difficult to do in general owing to the fact that δ depends specifically on the details of the experimental setup.

4. Experimental Setup

In this section we present different aspects of the experimental setup used to implement the alignment technique. The alignment setup must fulfill the following set of objectives: generate a wide, collimated, and monochromatic incident beam; minimize the value of β (the angle between the incident wave and the chip normal); provide a high-magnification image of the optical crosses and the alignment markers; and provide accurate and stable six-DOF positioning of the microlens-array substrate.

Two techniques were developed to achieve the above; they differ in their approach at minimizing the value of β. The first approach, based on the technique used in Ref. 32, uses the retroreflection of an incident wave from the surface of the chip to determine and minimize the value of β. The second ap-

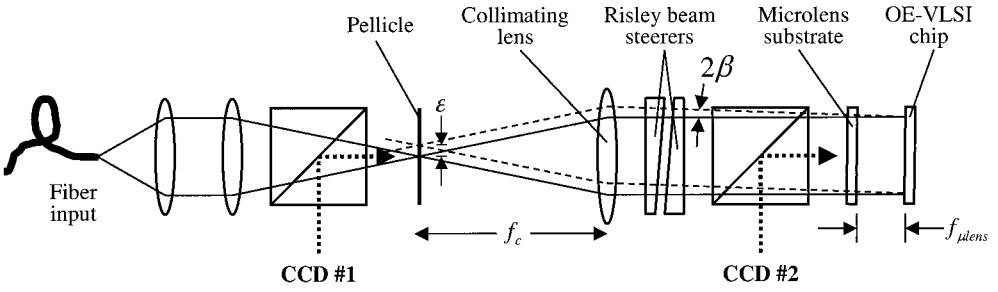

Fig. 5. Experimental setup that uses the retroreflected beam alignment technique.

proach is novel; it uses *in situ* alignment structures fabricated directly on the microlens substrate to control the orthogonality of the incident wave. What follows is a description and comparison of both techniques.

A. Retroreflected Beam Alignment Technique

This technique, previously used in Ref. 32, is described in Fig. 5. The optical train generates a beam of uniform irradiance that is collimated with a lens of focal length f_c. Collimation is optimized with a shear-plate interferometer. First, the chip is inserted and secured in place; the microlens substrate is not present at this point. As shown by the dotted lines in Fig. 5, the beam reflected from the chip is refocused by the lens and can be observed (with CCD camera #1) at the front focal plane in which a thin pellicle has been inserted. The pellicle is partially reflective; this allows for the retroreflected spot to be observed at the same time as the spot incident in the opposite direction. The pellicle is a few micrometers thick; this avoids undesirable ghost images of the spots. The use of a pellicle is preferred to the pinhole used in Ref. 32 because it allows for the retroreflected spot to remain visible even for large beam misalignments. Next, the Risley beam steerers are rotated until the retroreflected spot overlaps with the incident spot at the pellicle plane. At this point, the incident beam is orthogonal to the chip, and the value of β is minimized. The worst-case value of β is given by

$$\beta = \frac{1}{2}\arctan\left(\frac{\epsilon}{f_c}\right) \cong \frac{\epsilon}{2f_c}, \tag{6}$$

where ϵ corresponds to the decentration error involved in judging the alignment of the retroreflected spot relative to the incident spot. Approximation (6) remains valid regardless of the distance separating the collimating lens and the chip (i.e., the chip is not required to be one focal length away from the collimating lens). Next, the microlens substrate is attached to a six-DOF micropositioning stage and inserted in the optical train. Final alignment is obtained by registering the alignment targets of the microlens substrate to the optical crosses generated by the on-chip FZPs.

An important limitation of this technique is that it relies on the surface of the chip to be optically flat, which is not necessarily the case with standard CMOS chips. Furthermore, the addition of flip-chip OE devices on the CMOS chip further degrades the surface flatness. This translates into an aberrated retroreflected spot, leading to a large value of ϵ. To demonstrate this, the setup of Fig. 5 was constructed by use of a collimating lens with $f_c = 100$ mm and the OE-VLSI chip of Fig. 3. A photograph of the retroreflected spot in the plane of the pellicle appears in Fig. 6(a), showing a large amount of aberrations and a spot diameter of $\sim$120 μm. Taking the value of ϵ to be approximately equal to half the spot diameter, approximation (6) leads to a worst-case $\beta = 0.017°$. Next, the OE-VLSI chip was replaced with a 100% dielectric mirror with an optical flatness of $\lambda/10$. The resulting retroreflected spot, shown in Fig. 6(b), is much smaller with a diameter of $\sim$20 μm, leading

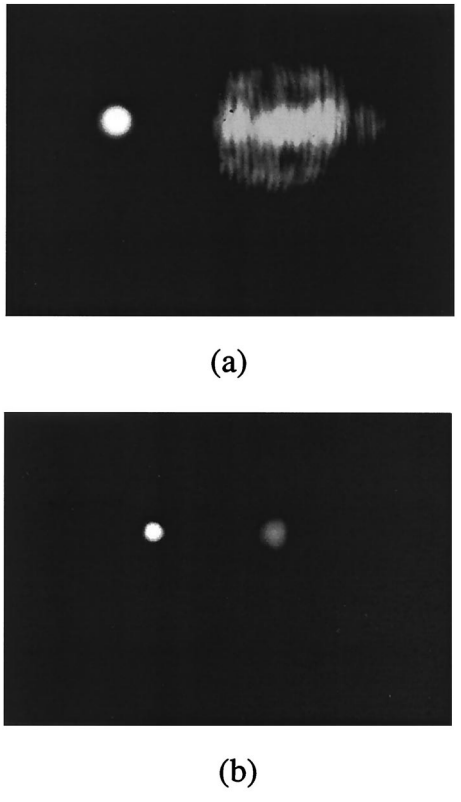

Fig. 6. Retroreflected spot from (a) the OE-VLSI chip of Fig. 3 and (b) a 100% mirror.

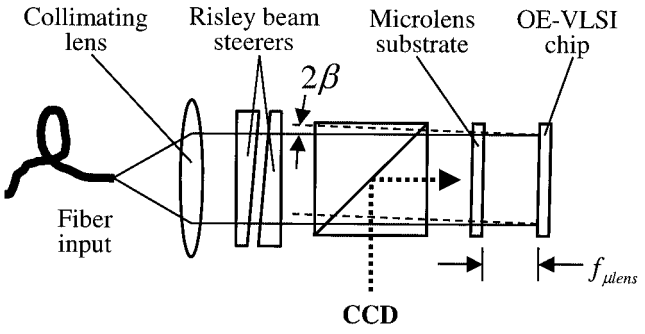

Fig. 7. Experimental setup that uses the *in situ* beam alignment technique.

to a worst-case $\beta = 0.003°$. This serves to illustrate how poor chip flatness can significantly affect the accuracy of the retroreflection technique. Although the accuracy can always be improved by further increases in the focal length f_c, this is done at the expense of a bulkier experimental setup.

B. *In Situ* Beam Alignment Technique

A new *in situ* alignment technique was developed to address the limitations of the previous method. A diagram of the optical train is shown in Fig. 7. First, the microlens substrate and the chip are both inserted in the setup. The chip is secured in place, and the microlens is attached to a six-DOF micropositioning stage. The next step consists of removing tilt misalignment between the microlens substrate and the chip. Tilt misalignment can be observed by use of the interference fringes produced by partial reflections from the microlens substrate and the chip surface, as shown in Fig. 8. This requires the use of a laser source with a coherence length that is at least two times longer than the distance separating the microlenses and the chip. Interference fringes are difficult to observe if the reflectivity of the microlens substrate is low, which is especially true if the substrate has been antireflection coated at the operating wavelength of the OE devices. To avoid this problem and increase the fringe contrast, it is often necessary to design and operate all alignment features at a distinct wavelength (e.g., a He–Ne laser at 633 nm). The amount of tilt misalignment ($\Delta\theta x$, $\Delta\theta y$) is determined by measurement of the fringe separation; this can be conveniently done by a count of the number of fringes, N, over a distance L along a line perpendicular to the fringe pattern. The tilt misalignment is given by

$$\Delta\theta x = \Delta\theta y = \arctan\left(\frac{N\lambda}{2L}\right) \cong \frac{N\lambda}{2L}. \tag{7}$$

For example, the fringe pattern in Fig. 8 shows 12 fringes (oriented at approximately 45° in the figure) over a distance of 2.2 mm, which translates in a tilt misalignment of 0.13° at $\lambda = 850$ nm. By carefully adjusting the tilt of the microlens substrate, one can easily bring the number of fringes down to 2 over the same distance, leading to a worst-case tilt misalignment of 0.022°.

Next, the incident beam is aligned orthogonal to the chip. This is achieved by use of dedicated linear FZPs fabricated directly on the microlens substrate, as shown in Fig. 9. The focal length of the linear FZPs is made equal to twice the separation between the microlenses and the chip, $f_{\mu\text{lens}}$. As a result, the incident beam is focused back into a line toward the center of the FZP. With this scheme, any angular deviation between the incident beam and the chip results in the decentration of the focal line relative to the FZP center. Risley beam steerers are adjusted until the focal line is properly centered on the FZP. To facilitate this adjustment, metal alignment targets are deposited in place of the central Fresnel zone. As shown in Fig. 9, two linear FZPs, oriented at 90° to each other, are required to perform θx and θy beam angular alignment. The worst-case angular deviation between the incident beam and chip is given by

$$\beta = \arctan\left(\frac{\delta}{2f_{\mu\text{lens}}}\right) \cong \frac{\delta}{2f_{\mu\text{lens}}}, \tag{8}$$

where δ corresponds to the error made in judging when the focal line is properly centered on the alignment targets. For the experimental setup described in Section 5, $\delta = 2$ μm and $f_{\mu\text{lens}} = 8.50$ mm, which results in $\beta = 0.0067°$. This is to be compared with $\beta = 0.017°$ obtained by use of the retroreflection technique and with $\beta = 0.09°$ obtained in Ref. 30. Comparison of approximations (6) and (8) shows that the *in situ* technique is more accurate than the retroreflection technique if $\delta/f_{\mu\text{lens}} < \epsilon/f_c$, which can be the case with a textured or nonplanar chip surface.

A significant advantage of the *in situ* technique is its ease of use; it allows for all of the misalignment information (angular deviation of the incident beam and the six-DOF misalignment of the microlenses) to be simultaneously monitored, in the same observation plane, with a single CCD camera. Additionally,

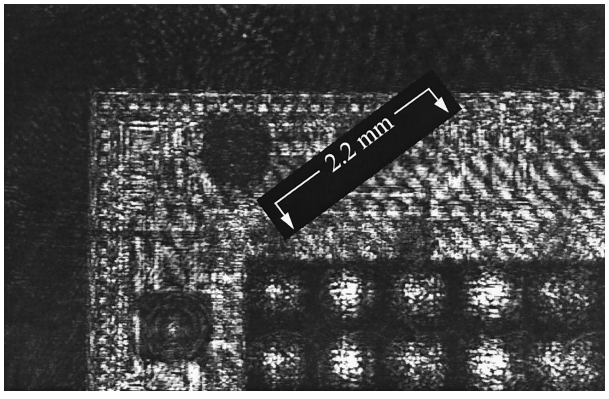

Fig. 8. CCD image showing interference fringes between the microlens substrate and the chip surface (only the upper-left corner of the chip is shown). The fringes are difficult to see owing to the low reflectivity of the microlens substrate; they are oriented parallel to the lines of the arrows.

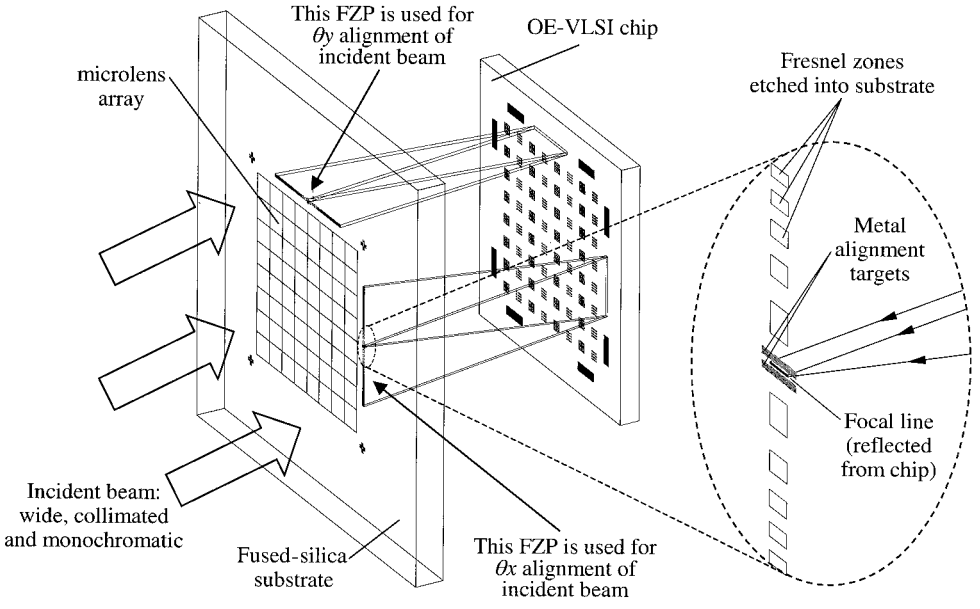

Fig. 9. Orthogonal beam alignment that uses *in situ* off-axis linear FZPs.

the *in situ* technique is more compact because it does not require the use of a long focal-length collimating lens.

5. Results

The alignment technique of Fig. 2 was used to package an 8×8 array of microlens to a 32×32 array of GaAs MQW modulators flip-chip bonded to a 9 mm $\times$ 9 mm CMOS chip. A photograph of the final package module is shown in Fig. 10. A complete description of the mechanical, thermal, and electrical design and testing of this module can be found in Ref. 11.

The alignment accuracy was determined through the use of Eq. (1) and approximations (2)–(4). For this design, the separation between the microlenses and the chip is $f_{\mu\text{lens}} = 8.50$ mm, and the distance between adjacent alignment targets on the microlens substrate is $d = 7150$ μm. The FZPs were designed with an off-axis angle $\phi = 8.90°$. The value of δ was determined experimentally to be 2 μm under $\times 50$ magnification. The worst-case misalignment error is calculated for both beam alignment techniques described in Section 4, and the results are compared in Table 1. The techniques differ mainly in their sensitivity to tilt misalignments. The results show that the use of interference fringes improves the tilt sensitivity by an order of magnitude. Overall, the *in situ* beam alignment technique is preferred because it is easier to use and more accurate.

An additional advantage of using off-axis linear FZPs, compared with on-axis circular FZPs, is that they consume less silicon area. For example, in the design of the module described in Ref. 11, each FZP could be made as small as 100 μm $\times$ 1000 μm. Assuming a pair of FZPs at each corner of the 9 mm $\times$ 9 mm chip, the area consumed by the FZPs represents less than 1% of the total silicon area. In comparison, four on-axis circular FZPs with the same

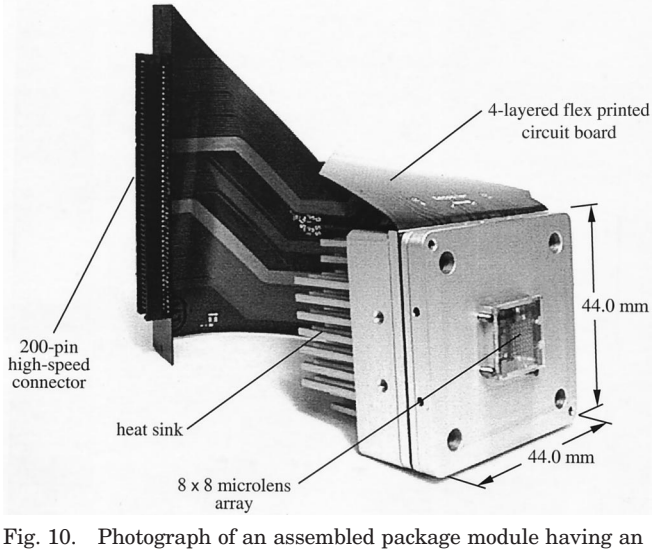

Fig. 10. Photograph of an assembled package module having an 8×8 array of microlens aligned to a 32×32 array of GaAs MQW modulators flip-chip bonded to a 9 mm $\times$ 9 mm CMOS chip.

Table 1. Worst-Case Misalignment Errors for Both Beam Alignment Techniques

Worst-Case Misalignment Error	Retroreflected Beam Technique (δ = 2 μm, ϵ = 50 μm)	*In Situ* Beam Alignment Technique (δ = 2 μm)
Beam Deviation (β)	0.017°	0.0067°
Lateral (Δx, Δy)	4.5 μm	3.0 μm
Rotational ($\Delta\theta z$)	0.023°	0.023°
Longitudinal (Δz)	13 μm	13 μm
Tilt ($\Delta\theta x$, $\Delta\theta y$)	0.20°	0.022°

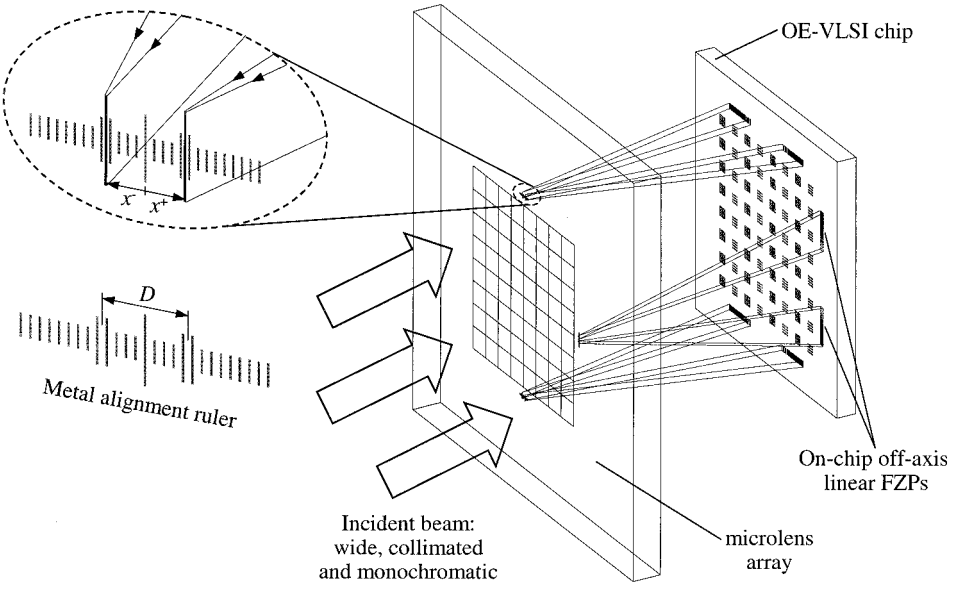

Fig. 11. Improved implementation of the six-DOF alignment technique.

f-number would consume 3.9% of the chip area, approximately four times more.

6. Discussion

The implementation of Fig. 2 was found to be awkward to use in practice because no alignment information could be inferred from measurements made on a single alignment target. For example, the decentration of a cross pattern may be caused by a lateral misalignment, a longitudinal misalignment, or a combination of both. This ambiguity can be resolved only by measuring the decentration of another cross pattern, located at the other corner of the chip. The consequence of this is that the operator is forced to travel back and forth between two alignment targets to determine the misalignment in one DOF.

This inconvenience has led to the proposal of an alternative implementation of the off-axis alignment technique, shown in Fig. 11. This implementation uses pairs of off-axis linear FZPs on each side of the chip that are combined with metal alignment features fabricated on the microlens substrate. As before, a wide, collimated, and uniform beam is incident orthogonal to the on-chip FZPs, and the light is reflected from the FZPs and focused into lines in the plane of the microlens array. In this case, the alignment features are designed as metal rulers and are used to measure the position and separation between two parallel focal lines: The separation between focal lines is a measure of longitudinal misalignment, whereas their position relative to the center of the metal ruler is a measure of lateral misalignment. The FZPs are designed such that perfect alignment of a metal ruler corresponds to a pair of focal lines that are separated by a distance D and symetrically positioned about the center of the metal ruler. The advantage of this type of layout is that both lateral and longitudinal misalignment information can be directly inferred from measurements performed on a single alignment feature. Defining x^+ and x^- to be the distance separating each focal line from the center of the horizontal metal rulers, the lateral (Δx) and longitudinal (Δz) misalignments of the metal ruler are calculated as follows,

$$\Delta x = x^+ - x^-, \tag{9}$$

$$\Delta z = \frac{x^+ + x^- - D}{2 \tan \phi}, \tag{10}$$

where ϕ is the off-axis angle defined in Section 3. By use of the definition of Eq. (10) and the implementation of Fig. 11, a positive value of Δz corresponds to the microlens substrate that is too close to the chip. Note that the lateral misalignment information from two alignment rulers located on opposite sides of the microlens array can be used to determine the rotational misalignment ($\Delta\theta z$) of the microlens. Similarly, the longitudinal misalignment information from three alignment rulers, located on different sides of the microlens array, can be used to determine the tilt misalignment ($\Delta\theta x$, $\Delta\theta y$) of the microlens substrate. Consequently, three alignment rulers, combined with three pairs of off-axis FZPs on the chip, are sufficient to determine the microlenses misalignment in all six DOFs.

The implementation of Fig. 11 can be further improved by placing the off-axis FZPs on the microlens substrate and the alignment features on the chip. The motivations for doing this are that (i) alignment features consume less silicon area than FZPs and (ii) FZPs implemented as multiple-phase-level lenses on the microlens substrate offer a higher diffraction efficiency. This arrangement also offers the possibility of using on-chip photodetectors to measure the position and separation of the focal lines, as shown in Fig. 12. In this implementation, the focal line pro-

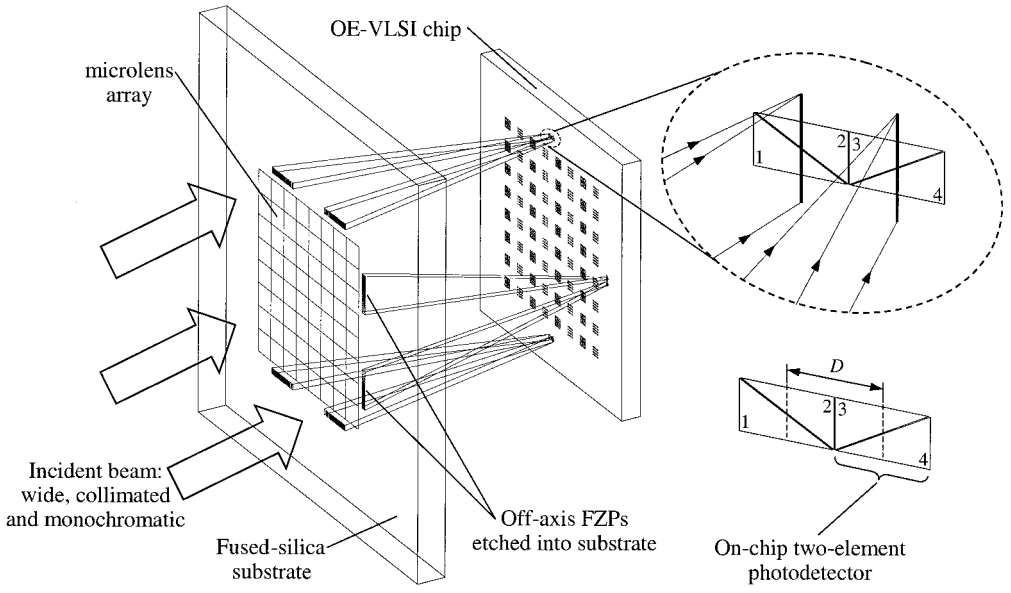

Fig. 12. Novel implementation that uses on-chip photodetectors to perform six-DOF alignment.

duced by one off-axis FZP on the minilens substrate is incident on a two-element photodetector on the chip. The active elements of the photodetector are triangular in shape, each element producing an equal photocurrent when the focal line is centered on the two-element photodetector. This type of photodetector may be implemented as CMOS-compatible p-n junctions.[33] The FZPs and photodetectors are designed such that, under perfect alignment, the focal line produced by each FZP is centered on its associated two-element photodetector. The four photocurrents (I_1, I_2, I_3, I_4) generated by a pair of two-element photodetectors are used to calculate both the lateral (Δx) and longitudinal (Δz) misalignments of that photodetector pair relative to the microlenses,

$$\Delta x = \left(\frac{I_2 + I_4 - I_1 - I_3}{I_1 + I_2 + I_3 + I_4}\right) D, \tag{11}$$

$$\Delta z = \left(\frac{I_1 + I_4 - I_2 - I_3}{I_1 + I_2 + I_3 + I_4}\right) \left(\frac{D}{2 \tan \phi}\right), \tag{12}$$

where D is the lateral dimension of a two-element photodetector along the direction perpendicular to the focal line. With previous arguments, it can be shown that three pairs of two-element photodetectors, for a total of 12 photocurrents, are sufficient to determine the chip misalignment in all six DOFs.

The main advantage of this implementation is the ease with which it can be automated by use of a closed-loop control system. To do this, the 12 photocurrent signals are transferred off-chip and measured by a computer equipped with an analog-to-digital converter card. Amplifying and filtering circuitry may be used off-chip to improve the signal-to-noise ratio. Equations (11) and (12) are then used to calculate the misalignment of the chip in all six DOFs. This information is used to control a six-DOF alignment stage holding to the chip. This approach is attractive because it can provide accurate six-DOF alignment in only a few seconds.

7. Conclusion

The realization of passively aligned 2D-FSOI systems relies on the development of cost-effective alignment techniques for assembling 2D array components, such as microlens arrays and OE-VLSI chips. This paper presents a novel six-DOF alignment technique that uses off-axis linear FZPs on one component combined with alignment targets on the other. The technique differentiates itself from previous techniques in that it offers accurate alignment in all six DOFs while not being limited to situations in which the components are close together.

The alignment is realized with an optical setup that generates a wide, collimated, and uniform incident beam orthogonal to the chip. An important source of error is due to the incident beam not being perfectly orthogonal to the chip. Two methods for minimizing this error were presented. The first method is a standard technique that uses the retroreflection from the surface of the chip to detect beam misalignment; its accuracy is limited by the surface flatness of the chip. The second method is novel; it avoids the limitations of the first by use of *in situ* off-axis FZPs and alignment targets fabricated directly on the microlens substrate to control the beam orthogonality.

The alignment technique was successfully used to package an array of diffractive microlenses with a 32×32 array of GaAs MQW modulators flip-chip bonded to a 9 mm $\times$ 9 mm CMOS chip.[11] With the *in situ* beam alignment method, the worst-case misalignment between the chip and the microlens is calculated to be $\Delta x = \Delta y = 3.0$ μm, $\Delta\theta z = 0.023°$, $\Delta z = 13$ μm, and $\Delta\theta x = \Delta\theta y = 0.022°$.

The original implementation of the alignment technique was found to be awkward to use in practice owing to the fact that no alignment information can be inferred from measurements performed on a single alignment target. This has led to the development of improved implementations of the off-axis alignment technique. We also propose the use of on-chip photodetectors to automate the alignment of the chip relative to the microlenses. This approach is attractive because it can provide accurate six-DOF alignment in only a few seconds.

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