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Electrical, thermal and optomechanical packaging of large 2D optoelectronic device arrays for free-space optical interconnects

M H Ayliffe†, D Kabal, F Lacroix, E Bernier, P Khurana, A G Kirk, F A P Tooley‡ and D V Plant

Photonic Systems Group§, McGill University, Department of Electrical and Computer Engineering, 3480 University St, Montréal, Québec, Canada H3A 2A7

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Abstract. Innovative approaches to the design of a high-performance package module accommodating a 32×32 array of surface-active devices indium bump bonded to a 8×8 mm^2 VLSI chip are presented. Electrical, thermal and optomechanical design considerations are discussed and experimental performance results of a prototype implementation are described. The package module supports 139 impedance-controlled signal connections as well as active temperature stabilization of the optoelectronic VLSI chip. The package module is compact, simple to assemble, alignment-tolerant and can be passively inserted into a free-space optical system with no need for further adjustments.

Keywords: Optoelectronic packaging, free-space optical interconnect, 2D array, passive alignment, optomechanics

1. Introduction

Free-space optical interconnects (FSOIs) utilizing two-dimensional (2D) optoelectronic device arrays hold the promise of solving the bandwidth bottlenecks of future computing and telecommunications switching systems. However, today's most important obstacle to the acceptance of FSOIs in commercial applications has to do with the cost and manufacturability of the optical and optomechanical components and whether the employed packaging techniques are amenable to low-cost and high-volume manufacturing [1].

Providing an integrated packaging solution for a 2D array of surface-active devices presents a series of electrical, thermal and optomechanical requirements. Specifically, a successful packaging solution must:

- Provide a large electrical connectivity to the optoelectronic VLSI (OE-VLSI) chip.
- Provide high-speed signal lines operating at hundreds of Mbit s^{-1}.
- Allow for temperature stabilization of the OE-VLSI chip.
- Meet a predetermined set of alignment tolerances dictated by the interconnect design.
- Be mechanically and thermally stable to withstand the rigours of commercial installations.
- Allow for simple assembly and low-cost alignment packaging techniques.
- Allow for field-serviceability of the OE-VLSI chip (i.e. being able to replace defective chip modules without having to realign the optical system).

This paper describes the design considerations and provides experimental performance results of a package module accommodating a 32×32 array of GaAs/AlGaAs quantum confined Stark effect (QCSE) devices indium bump bonded to a 8×8 mm^2 VLSI CMOS chip. This OE-VLSI chip is to be part of a four-stage optically distributed photonic backplane system interconnecting processing elements located on individual electrical printed circuit boards. A detailed description of the concept, motivation and design of a photonic backplane can be found in [2]. A detailed description of the optical interconnect design, as well as the constraints and trade-offs that led to its development, can be found in [3]. The optical interconnect design is based on telecentric relays of 8×8 arrays of mini-lenses (defined as a lens with ∼0.5–2.0 mm diameter supporting a small 2D cluster of beams, in contrast with a 'microlens'—being a smaller lens supporting a single beam). Each mini-lens has a diameter of 800 μm and a focal length of $f = 8.5$ mm. The

† E-mail address: mikea@photonics.ece.mcgill.ca
‡ Previously with the Electrical and Computer Engineering Department at McGill University; now with the Department of Physics at Heriot-Watt University, UK.
§ Webpage http://www.photonics.ece.mcgill.ca.

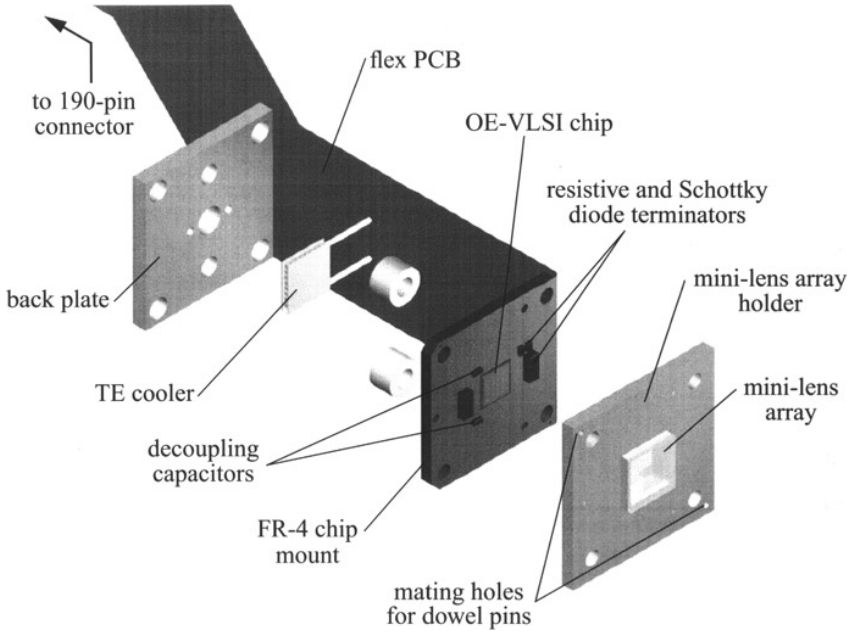

Figure 1. Exploded view of the package module.

QCSE devices are arranged in an 8×8 array of clusters, every cluster consisting of a 4×4 array of modulator or detector devices (for a total of 1024 devices occupying a region of 6.4×6.4 mm^2 on the chip).

2. Package module description

Partitioning a large-scale FSOI system into separate modular subassemblies greatly reduces the assembly complexity and facilitates future servicing of the system. Accordingly, it is useful to consider the OE-VLSI chip and its associated components as part of a package module which can be independently assembled, aligned and tested prior to its final integration with the optical system.

An exploded view of the package module design is shown in figure 1. The design integrates a mini-lens array, an OE-VLSI chip, a flexible printed circuit board (flex PCB) and a thermoelectric (TE) cooler. The OE-VLSI chip is directly attached to a custom-designed 3.175 mm thick FR-4 mount (fabricated using standard PCB manufacturing techniques [4]). This mount primarily acts as a rigid support structure for the chip and has no electrical functionality. The custom-designed two-layer flex PCB is glued onto the mount using high-temperature thermal set lamination techniques. The chip is then wirebonded directly to gold-on-nickel plated printed circuit using an aluminium wedge wirebonder. This integrated packaging approach offers a number of distinct advantages, none of which are available with standard consumer electronic carriers and packaging techniques. First, the flex PCB offers greater design freedom in the routeing of the electrical connections coming off the chip such as to minimize the footprint of the module while providing high-speed impedance controlled traces with terminations in close proximity to the chip. Second, the FR-4 chip mount represents a low-cost integrated support structure capable of providing thermal vias, lithographically defined metal alignment marks and high-precision machining of through holes. A photograph of a completely assembled package module (including a close-up of the PCB flex with the mini-lenses removed) is shown in figure 2.

3. Electrical packaging design and characterization

In order to support the bandwidth and connectivity requirements of a large digital electronic system, the electrical packaging design is required to:

- Provide 139 signal connections (not including power supply and ground connections) from the OE-VLSI chip to the associated printed circuit board of the electronic system.
- Effectively terminate 32 high-speed inputs (5V NRZ at a target bit rate of 100 Mbit s^{-1}) and two clock signals (5V NRZ at a target frequency of 320 MHz).
- Provide impedance control for the high-speed inputs and for the two clock signals.
- Minimize the amount of crosstalk between adjacent lines.
- Provide power supply decoupling to reduce noise.
- Mechanically isolate the package module from the electronic system.

What follows is a brief description of the electrical characteristics of the package, showing how the design successfully addresses the above requirements. The flex PCB is 150 μm in thickness and has two copper layers; its very high flexibility ensures mechanical isolation of the package module from the optical system. The top copper layer has high-speed traces and the back layer is a ground plane, allowing for a microstrip stackup with a 50 μm dielectric thickness. The signal traces are 100 μm in width and 17.8 μm in thickness. Using the electromagnetic field solver built into the CAD tool package, the calculated impedance of this

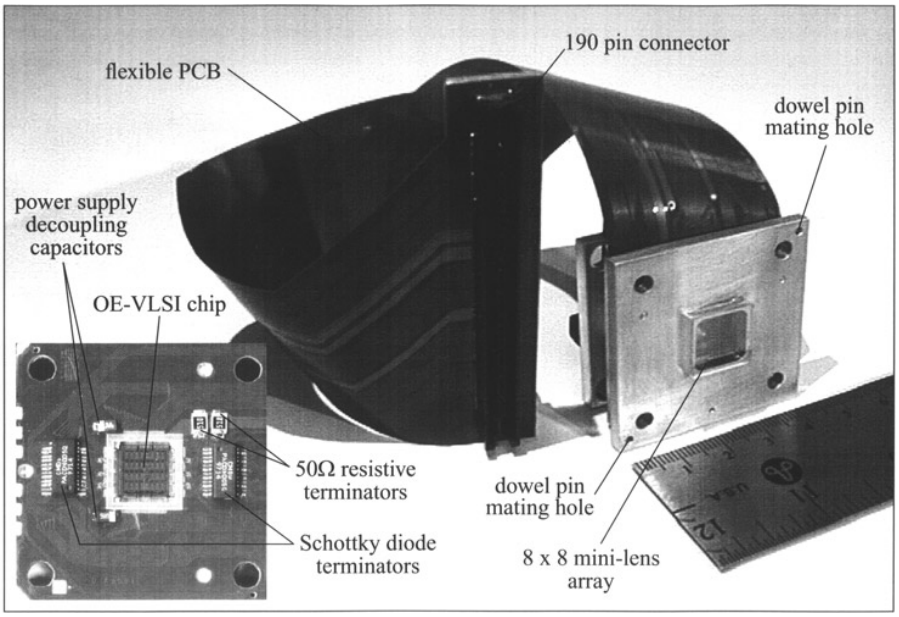

Figure 2. Photograph of an assembled package module.

microstrip is 50 Ω and the worst-case estimated coupled crosstalk between adjacent lines is 0.1 V. The signal lines have a 200 μm pitch, allowing for all 139 signal connections to be routed from the periphery of the chip to a 190 position connector with an integral ground plane and 50 Ω impedance control. The resulting footprint of the package module is 40 mm × 40 mm.

The input pads on the chip are standard high impedance CMOS pads, necessitating external 50 Ω resistor terminations for the two 320 MHz clock signal lines. For the 32 high-speed inputs running at 100 Mbit s^{-1}, resistive termination of all signal lines was prohibitively large in footprint; active termination using Schottky diode terminators was used instead. This approach is independent of the line characteristic impedance as the diode terminators are designed to prevent only excursions from the power supply rails. Two power supply decoupling capacitors were also mounted on the flex PCB immediately adjacent to the chip. Individual trace performance was measured using time domain reflectometry and Smith chart features of a network analyser, showing an average characteristic impedance of 50 Ω with a worst-case 20% peak deviation. The resistance of the traces, measured from the connector to the chip, was less than 5 Ω. Over the same distance, the signal propagation delay was measured to be 2 ns.

4. Thermal packaging design and characterization

An upper bound for the total expected power consumption of the chip was estimated to be 5 W. Based on experimental characterization data from the QCSE devices, it was determined that the combined modulator/detector performance characteristics of the QCSE devices were optimized for a chip operational temperature between 40 and 50 °C [5]. With an expected power dissipation of 5 W, setting the temperature of the chip within the allowable operation window requires active temperature control and stabilization techniques. Experiments were conducted to determine the thermal efficiency of the package design. A thermoelectric (TE) cooler was mounted to the back of the FR-4 mount and a thermistor was attached to the back of the same mount with one end connected to the thermal vias. The experiments consisted in replacing the chip with a 5 W dissipating resistor and using the TE cooler to stabilize the temperature at a fixed point between 40 and 50 °C. It was found that the steady-state temperature with the TE cooler off was only about 40 °C, indicating the need for operating the TE cooler towards heating the chip, which could be achieved with a resolution of 0.01 °C.

Table 1. Package module alignment tolerance analysis.

Degrees of freedom	Mini-lenses packaged with chip	Mini-lenses packaged with optical system
Lateral (x, y)	±26 μm	±8 μm
Longitudinal (z)	±500 μm	±125 μm
Tilt (Θ_x, Θ_y)	±0.03°	±0.12°
Rotational (Θ_z)	±0.36°	±0.10°

5. Optomechanical design and characterization

An important feature of the design is the integration of a mini-lens array substrate as part of the package module. An alternative choice would have been to package the mini-lens array into the adjacent optical system. The alignment tolerance analysis comparing these two options is shown in table 1. This analysis calculates the amount of individual misalignment (for each degree of freedom) that could occur before the optical power throughput in the interconnect drops to 99% of the value for a perfectly aligned system.

The results indicate that integrating the mini-lens array with the OE-VLSI chip relaxes the x, y, z and Θ_z alignment tolerances by a factor of about four (this intuitively makes sense since the surface-active devices look bigger when

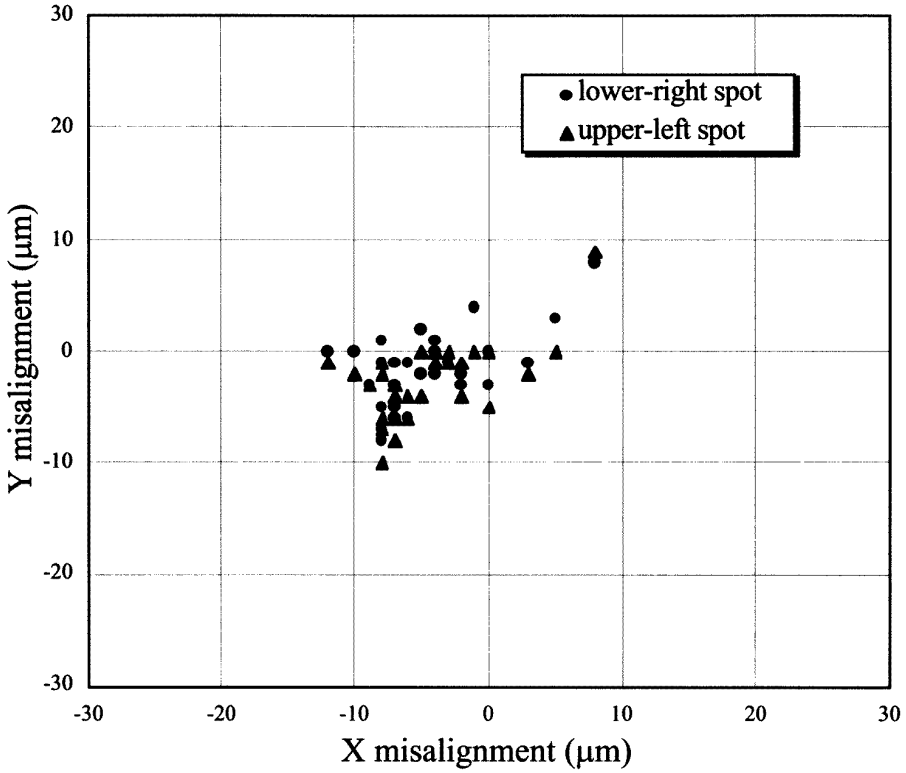

Figure 3. Results of the package module repeatability tests.

viewed through the mini-lens array) but tightens the Θ_x and Θ_y alignment tolerances of the package module by approximately the same amount (due to the optical lever arm effect of the mini-lenses). The results of table 1 illustrate how the assembly and alignment of the mini-lens array to the OE-VLSI chip is a key technology.

Whenever possible, passive alignment of optical subassemblies is preferred to active alignment because of its greater manufacturability. For this reason, several different passive alignment schemes were investigated; in all cases, the cumulative dicing, machining and locational tolerances exceeded the allowed misalignment (as specified in the second column of table 1), indicating the need for an alternative alignment technique in this case. Active alignment schemes suitable to our application have been demonstrated in the past (see, for example, [6]). Although these packaging techniques were used successfully to produce high-performance optical subassemblies, they are labour intensive and generally require a high level of operator skill. For this reason, a novel alignment technique has been proposed and is currently being implemented. The technique uses alignment reference beams with on-chip detectors to precisely detect the misalignment of the mini-lenses in all degrees of freedom. The technique is accurate and offers the potential of being fully automated, thereby avoiding the drawbacks generally associated with active alignment schemes.

One critical design objective was to give the package module the ability of being passively inserted into the optical system without requiring further adjustments. The proposed interface design uses two precision-ground dowel pins that mate with the lens array holder (accounting for the x, y and Θ_z degrees of freedom) and utilizes the well-defined planar front surface of the mini-lens array substrate as a passive alignment reference that can adequately satisfy the $\pm 0.03^\circ$ tilt requirement.

This design approach was validated by inserting a dedicated package module into a prototype optical system and illuminating it with an array of 512 spots delivered from an optical power supply delivery system [7]. The module was then removed, inserted back and secured in place. This step takes about 15 s and was repeated 30 times. For every extraction/insertion cycle, the x–y misalignments of the two spots located at the opposite corners of the array were recorded. The repeatability measurements are shown in figure 3. The results indicate that this package module can be passively inserted into an optical system with all spots in the array being properly aligned to within ± 12 μm in both lateral directions. Thus, by making the active area of the QCSE devices larger than the spot size by the latter amount, the OE-VLSI chip can be manually inserted into the optical system with zero insertion loss and no need for further adjustments. This result is significant because it demonstrates the ability of large array (>1000 devices) OE-VLSI chips to be field-serviceable, a pre-requisite for FSOI systems to become a commercial reality.

6. Conclusions

The design of a high-performance FSOI package module was presented. The module integrates an 8×8 mini-lens array, an OE-VLSI chip with 1024 QCSE devices, a flexible printed-circuit board supporting 139 impedance controlled

signal connections and a TE cooler to adequately stabilize the operating temperature of the chip. It was shown that the package module can be passively inserted in a FSOI system with no need for further adjustments, demonstrating the ability of high-capacity OE-VLSI chips to be field-serviceable.

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