Design, Modeling, and Characterization of FET-SEED Smart Pixel Transceiver Arrays for Optical Backplanes

David V. Plant, *Member, IEEE,* Alain Z. Shang, Marcos R. Otazo, David R. Rolston, Brian Robertson, and H. Scott Hinton, *Senior Member, IEEE*

***Abstract*—The design, modeling, and characterization of FET-SEED Smart Pixel transceiver arrays fabricated for application in optical backplanes are presented. Results of digital and analog measurements on 4 × 4 transmitter arrays and 4 × 4 receiver arrays, packaged at the printed circuit-board level, will be presented. In addition, these results will be compared to device and circuit models developed for these optoelectronics. Finally, the description of the successful application of these optoelectronics to interconnect two printed circuit boards will be described.**

I. Introduction

FUTURE digital systems such as ATM switching systems and multiprocessor computer systems will have large printed-circuit-board (PCB)-to-printed-circuit-board connectivity requirements to support the large aggregate throughput demands being placed on such systems. Current electronic technology may not be capable of supporting both the connection densities and the bandwidth required due to limitations of multipoint electrical connections over backplane distances [1]. Free-space optical interconnects represent a potential solution to the needs of these connection-intensive digital systems. When implemented at the PCB-to-PCB level in the form of an optical backplane, this technology is potentially capable of providing greater connectivity at higher data rates than can be supported by current or projected electronic backplanes [2].

An optical backplane can be constructed using two-dimensional (2-D) arrays of passive, free-space, parallel optical-communication channels which optically interconnect PCB's via smart pixels arrays. The smart pixel optoelectronics are 2-D device arrays capable of electrical-to-optical (E/O) and optical-to-electrical (O/E) conversion of digital data. In addition to the E/O and O/E conversion, these devices can perform processing operations at the backplane level such as address recognition or packet routing. By interconnecting PCB's with 10 000 channels per board (10 smart pixel arrays per 1000 smart pixels per SPA or 2000 communication channels), each channel running at 100 Mb/s will support greater than a Tb/s of aggregate data traffic.

The identification of critical research issues in free-space optical systems is being pursued in the form of system demonstrator experiments [3]–[7]. With this objective in mind, we have designed, modeled, and characterized FET-SEED transceiver arrays for application in optical backplane demonstrators. This paper is organized as follows. Section II discuses the transceiver circuit design and fabrication, Section III the device and circuit models, and Section IV the PCB-level packaging of the circuits. Next, Section V will describe measured and modeled circuit performance of the modulator arrays, and Section VI will describe both optical and electrical measurements of the receiver circuits, including the associated model-predicted performance. Section VII will describe a unidirectional bulk optics-based interconnection of two PCB's which implement these device arrays, and Section VIII will conclude.

II. FET-SEED Transceiver Circuit Design

Arrays of individually addressable FET-SEED transmitters and receivers were fabricated using the batch-fabrication process made available through the ARPA—Consortium for Optical and Optoelectronic Technologies for Computing (CO-OP) and AT&T [8]. The FET-SEED technology monolithically integrates 1-μm gate length GaAs field-effect transistors with normal-incidence multiple-quantum-well (MQW) modulators and detectors to form a smart pixel [9]. Using this technology, we designed a 4 × 4 array of electrically addressable, amplified differential modulators, and a 4 × 4 array of diode-clamped, optical receivers with off-chip drivers [10]. Fig. 1 shows a layout of the chip. The transmitter array is located in the upper left corner, and the receiver array is located in the lower right corner. In both arrays, the optical windows had dimensions of 25 × 25 μm, were separated by 50 μm, and pitched at 200 μm. The transmitter circuit operates by electrically modulating the voltage drop across the series MQW diode pair, subsequently modulating the reflectivity of the diodes [11]. Both the load and switching MESFET transistors were 25 μm wide. The receiver circuit shown in Fig. 2 operates by demodulating dual-rail optical signals which are detected

Manuscript received June 5, 1995; revised February 29, 1996. This work was supported in part by the BNR-NT/NSERC Chair in Photonics Systems, the Canadian Institute for Telecommunications Research, NSERC (#OPG0155159), FCAR (#NC-1415), and the McGill University Graduate Faculty.

D. V. Plant, A. Z. Shang, M. R. Otazo, D. R. Rolston, and B. Robertson are with the Department of Electrical Engineering, McGill University, Montreal, PQ H3A 2A7 Canada.

H. S. Hinton was with the Department of Electrical Engineering, McGill University, Montreal, PQ H3A 2A7 Canada. He is now with the Department of Electrical and Computer Engineering, University of Colorado, Boulder, CO 80309 USA.

Publisher Item Identifier S 0018-9197(96)05587-X.

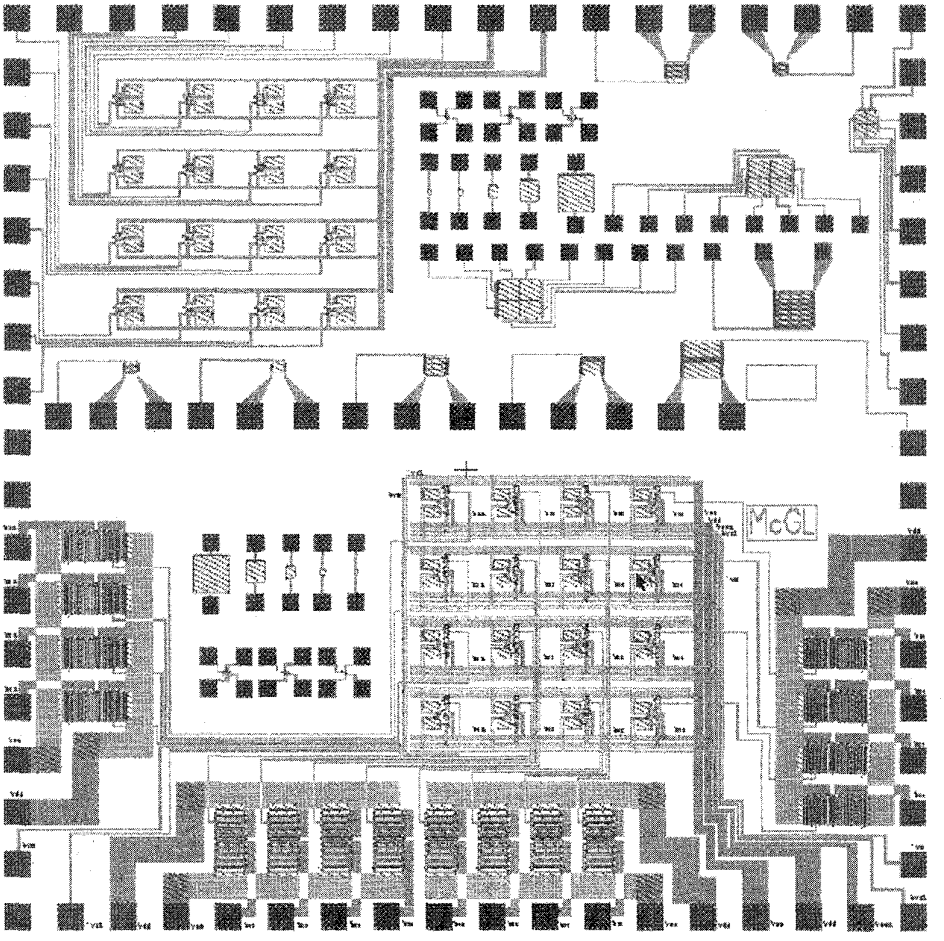

Fig. 1. Photograph of FET-SEED Chip showing 4 × 4 transmitter array (upper left-hand corner) and 4 × 4 receiver array (lower right-hand corner). Additional devices are shown including test FET's and diodes used to measure device dc characteristics.

using a series-connected detector-diode pair to form a diode-clamped receiver [12]. The input node to the first FET is charged and discharged as a function of the state of the incident optical power. The demodulated optical signal drives a three-stage amplifier circuit. The first two stages form a series pair of inverters with a total of four load and active transistors, each transistor being 6 μm wide. The third stage (shaded) is a 375-μm power FET designed to drive 100-Ω transmission lines.

In addition to the 4 × 4 arrays, individual FET's, PIN junction diodes, and Schottky diodes were included on the die for dc probing purposes. The I–V curves of these discrete devices were measured and the data was used to develop device models. The modeling of these devices and circuits will be described in the next section, followed by a description of the packaging and performance of the devices in the following sections.

III. Device and Circuit Models

The FET-SEED circuits were simulated using Microsim PSPICE version 5.4 [13]. The FET characteristics were modeled with the Raytheon model for GaAs MESFET's [14], [15]. Fig. 3 shows a fit of the model-generated I–V curves and those obtained experimentally. Typical measured dc currents of the transistors at $V_{gs} = 0$ V were 75.5 mA/mm at $V_{ds} =$ 2.0 V, and the measured transconductance at $V_{gs} = 0$ was 93.5 mS/mm. The measured threshold voltages were -1.2 V, and the drain-source breakdown voltages were greater than 8 V The MESFET current gain bandwidth, f_t, was calculated using $g_m/2\pi(C_{gs} + Cgd)$, where g_m is the model predicted FET transconductance, and C_{gs} and C_{gd} are the modeled gate-source and gate-drain capacitances, respectively, at the operating point of the MESFET. Using values of $C_{gs} = 9.51$ fF and $C_{gd} = 1.1$ fF [16], we calculated an fF of 13.5 GHz, which is in good agreement with an experimentally measured f_t of 10 GHz [17]. The diode modeling (Schottky diodes and PIN junction diodes) was done using the standard PSPICE-based model for diodes.

In addition to FET's and diodes, we also modeled the trace lines and the bond pads. The trace lines were modeled as RLC distributed networks with characteristic impedance Z_o, resistance R_o, inductance L_o, and capacitance C_o per unit length. The values of these parameters were calculated assuming a conventional microstrip geometry for metal interconnects [18]. For the FET-SEED technology, the metal interconnects are

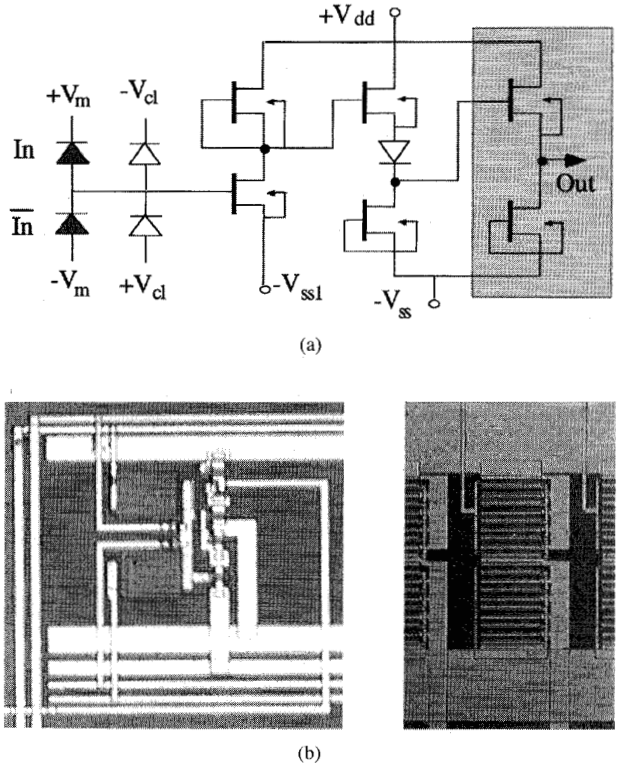

Fig. 2. (a) Receiver circuit schematic. (b) Photograph of the an individual receiver circuit, with insert showing power FET.

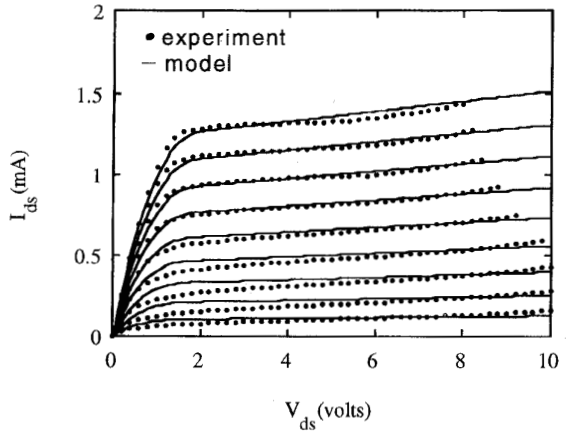

Fig. 3. Measured and modeled dc I–V curves for 10 μm MESFET (-1.0 V $\leq V_{gs} \leq +0.6$ V, 0.2-V steps).

300-nm-thick gold with $\rho = 2.2 \times 10^{-16}\,\Omega$ cm. The receiver signal interconnects are 4 μm wide and the transmitter signal interconnects are 5 μm wide. The parameter values of the RLC distributed model were calculated to be $R_o = 0.0183$ Ω/cm, and $C_o = 0.5492$ pF/cm $L_o = 14.26$ nH/cm. For the 75 μm$\times$ 75 μm bond pads, the loading capacitance was calculated to be 13.85 fF. Using these models for the devices and metal interconnects, the high-frequency performance of both the transmitter and the receiver circuits was calculated and correlated to experimentally measured performances. The results of these measurements and associated correlations will be described in the next three sections.

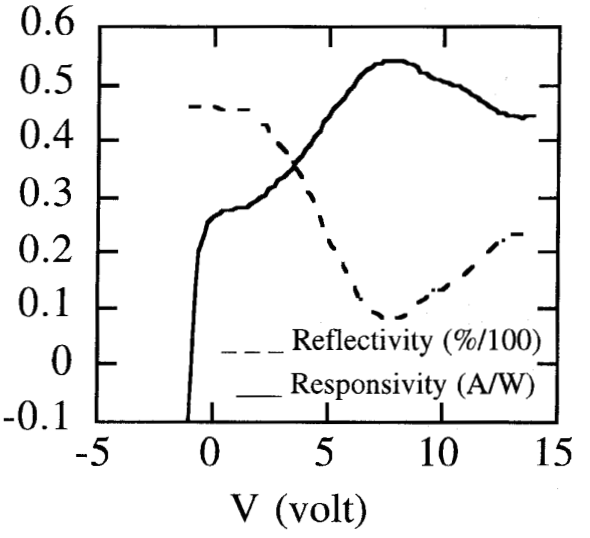

Fig. 4. Typical responsivities and reflectivities of the SEED diodes versus voltage at 850 nm.

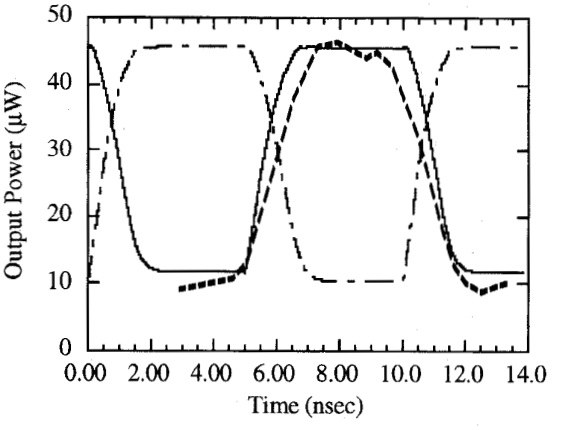

Fig. 5. Typical experimentally measured (solid) and modeled (dashed) reflectivity change of a modulator driven at 1 GHz with a peak-to-peak voltage of 2.0 V. The average (over 16 circuits) experimentally measured rise times of the circuit, after deconvoluting the appropriate detector response, was $t_{\mathrm{rise,avc}} = 0.84$ ns at $V_g = 2.0$ V.

IV. FET-SEED Transceiver Packaging

The FET-SEED transceiver circuits were wire bonded into high-speed multilayer ceramic quad-flat packages (QFP) capable of carrying forty signals with 2:1 signal-to-ground ratios. These packages were further integrated onto PCB's using a pressure-based, solderless disconnect which had 50-Ω impedance-matching capabilities. By appropriately tuning the package to board impedance, these QFP/PCB packages were capable of supporting forty 3-GHz signal lines. In order verify the bandwidth properties of these packages, network analyzer measurements were conducted on the assemblies. The 3-dB point of the QFP/PCB assembly was measured to be greater than 3 GHz, with a 0.1-dB transmission loss over the 5 KHz–100 MHz range. All optical and electrical measurements of the FET-SEED electronics described in the following sections were performed on devices packaged at the PCB level using these assemblies.

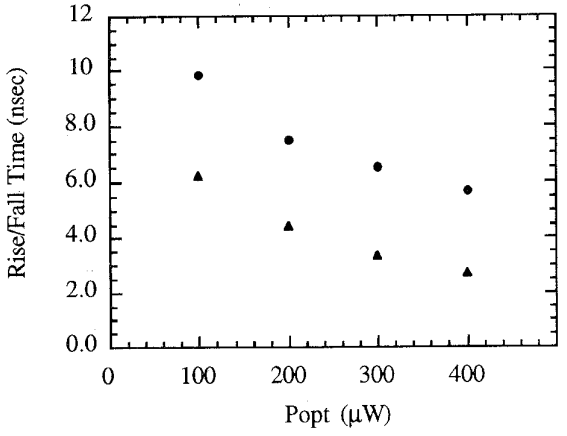

Fig. 6. Experimentally measured rise times (triangles) and fall times (circles) versus optical input power of the diode clamped receiver when driven by an externally modulated laser with a 200-ps rise time. The fastest rise time was 2.7 ns.

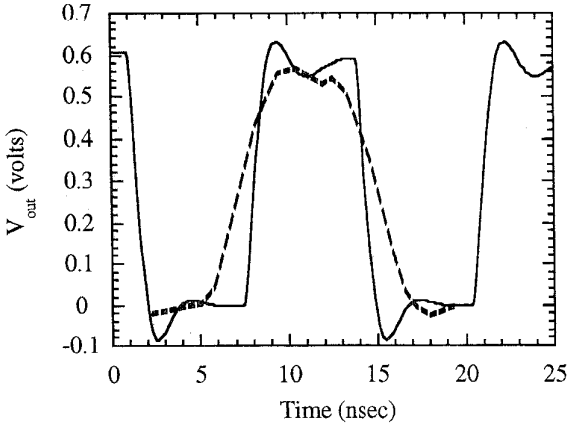

Fig. 7. Output of a received pixel, experimentally measured (solid) and modeled (dashed) when driven by a square wave with a 150-ps rise time. Typical measured rise times were 2.87 ns.

V. Modulator-Array Characterization and Comparison to the Model

The optical properties of the modulators and the detectors were measured using an 850-nm source, the λ_1 operating point for these SEED structures. Fig. 4 shows a plot of the typical diode responsivity and reflectivity versus voltage at 850 nm. Individual modulators exhibited a reflectivity change of 3 to 1 with -7.5 V of applied bias, and modulator pairs in the transmitter circuit exhibited a 2 (60%) to 1 (30%) reflectivity contrast ratio. The detectors had a responsivity of 0.5 A/W.

High-frequency measurements were performed on the transmitter circuits by applying 400-Mb/s digital signals to the gate of the switching transistor. Individual optical beams were used to read out the state of the modulator pair, the reflected light being focused onto a fast photodiode ($t_{\text{rise}} = 21$ ns) to monitor the switching speed. For these measurements, the 4×4 array was biased at $V_{dd} = 7.3$ V and V_{ss} grounded, and the incident power on the transmitter modulators was 290 μW. The 400 Mb/s input signal was applied at two voltages, 1.0 and 2.0 V

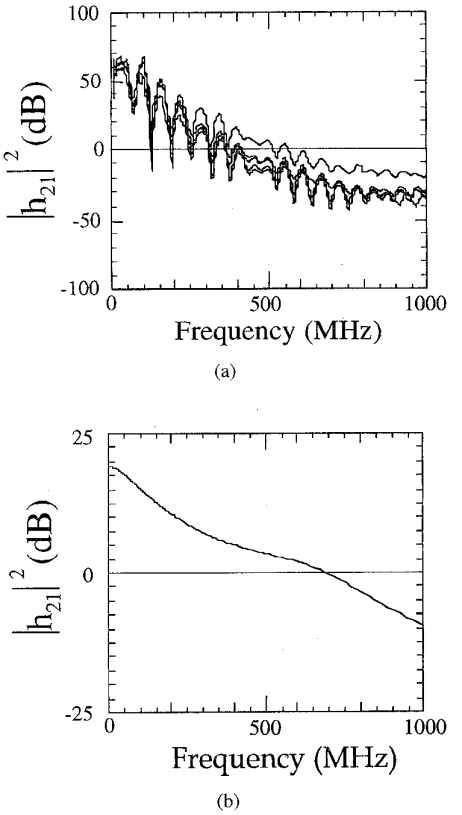

Fig. 8. (a) Experimentally measured h_{21} values of five receiver pixels derived from S parameters (b) and model-predicted performance.

peak-to-peak. The average (over 16 circuits) experimentally measured rise times of the circuit, after deconvoluting the appropriate detector response, were $t_{\text{rise,ave}} = 1.22$ ns, and $t_{\text{rise,ave}} = 0.84$ ns at $V_g = 1.0$ V, and 2.0 V, respectively. The 3-dB bandwidths, calculated using $f_{3\text{dB}} = 2.2/2t_{\text{rise}}$, were found to be $f_{3\text{dB}} = 291.55$ MHz, and $f_{3\text{dB}} = 431.65$ MHz at $V_g = 1.0$ V and 2.0 V, respectively, and the unity gain bandwidth was determined to be $f_o = 1.51$ GHz, and $f_o = 2.04$ GHz, assuming an output swing of 7 V and input swing of $V_g = 1.0$ V and $V_g = 2.0$ V, respectively. These measurements are in close agreement with values obtained by Lentine *et al.* [11] The rise times presented in this paper are approximately three times larger than those of [11], primarily due to the larger modulator size (25×25 μm versus 10×10 μm). Using the model described by Lentine *et al.*, it can be shown that the rise time is given by CV_o/DI_{FET} (if photocurrent is ignored) where C is the total capacitance, V_o is the output voltage across a MQW, and DI_{FET} is the difference in current between the load and switching transistors as the output begins to change state. The capacitance in this experiment was approximately 12 times greater due to the larger modulators, but the difference in current was approximately four times larger owing to the fact that the transistors were equally sized. Combining these two differences, we expect the rise time to be approximately three times larger than [11], as was measured.

This circuit was modeled using the above device and interconnect models. Fig. 5 shows both the experimentally

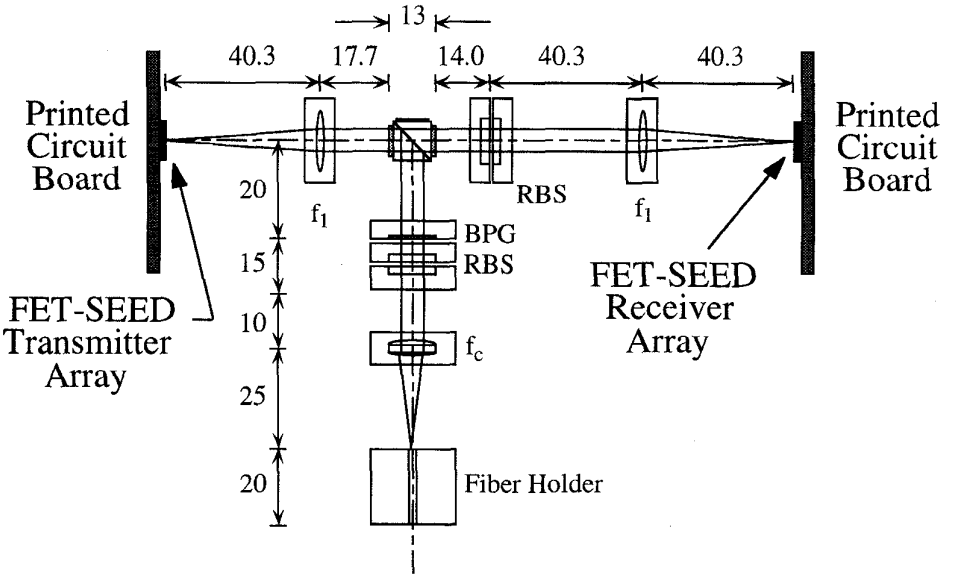

Fig. 9. A board-to-board optical interconnection constructed using a two-sided optical backplane approach and polarizing optics for beam steering.

measured (solid) and modeled (dashed) reflectivity change of a modulator driven at 1 GHz with 2.0 V peak-to-peak drive voltage. In addition to the electronics, we modeled the SEED devices with a current source in parallel with a capacitance. The current source depended linearly on the optical power, thus the *I–V* characteristic could be described using a simple look-up table [19], and the capacitance was assumed to be 0.115 fF/μm^2 [20]. The transmitter was simulated with a 100-μW optical input on both modulators. Based on this model, the predicted rise times where as follows: $t_{\rm rise} = 1.14$ ns for $V_g = 1.0$ V, and $t_{\rm rise} = 0.68$ ns for $V_g = 2.0$ V. Using these values, we predict 3-dB bandwidths of $f_{\rm 3dB} = 307$ MHz and $f_{\rm 3dB} = 515$ MHz, and unity gain bandwidths of $f_o = 1.535$ GHz and $f_o = 1.648$ for $V_g = 1.0$ V and 2.0 V, respectively. As can be seen, these results are in good agreement with the experimentally measured circuit rise times, 3-dB bandwidths, and unity gain bandwidths cited above.

The array was also tested for electrical cross talk in order to measure the electrical isolation between adjacent on-die trace lines. This measurement was performed by driving one transmitter circuit and measuring the voltage cross talk on the adjacent addressing trace line. A 2.0-V square wave was applied to a transmitter, and this transmitter's nearest neighbor input was monitored using a 50-Ω terminated digitizing scope. Twenty-mV spikes were induced by these addressing signals. We attribute this voltage cross talk to parasitic cross talk in adjacent signal lines. Similar measurements were performed on next-nearest neighboring lines, but no detectable voltage cross talk was found.

VI. Receiver–Array Characterization and Comparison to Model

Both optical and electrical, high-frequency receiver-circuit measurements were performed and compared to the predicted performance. In the case of the optical measurements, modulated light was focused onto one optical window of the receiver differential pair. The source of modulated light was an 8-GHz electrooptic modulator, which was driven by a digital stimulus system with a rise time of 150 ps. The output of the electrooptic modulator was measured using a fast photodetector, and the rise time was measured to be 200 ps, with a contrast ratio of 13.98 dB.

Using this source, the rise and fall times of the receiver circuit were measured. The optical power for the high state (beam-on) was varied from 100 μW to 400 μW, corresponding to switching energies between 69 fJ/b and 100 fJ/b. The results of the measurements are shown in Fig. 6, with the fastest rise time being 2.7 ns. The longer fall times were due to the fact that only one beam was used to drive the receiver. When the beam is on, the input node of the receiver is pulled to its clamping voltage, giving the fast rise time. When the beam is off, the input discharges to the beam-off voltage. If the channel were operated differentially, the discharge would be faster because an optical input would pull the input node to its opposite clamping voltage, thus yielding a faster fall time.

The high-frequency electrical measurements could be accomplished owing to the fact that the devices were packaged using high-bandwidth signal lines for dc biasing. Using a bias tee, the clamping diodes could be biased to their optimum operating point, and then either digital or analog signals could be applied to the input transistor of the three-stage amplifier. Because all the clamping diodes on the die are electrically tied to two inputs (one for $+V_{cl}$ and one for $-V_{cl}$), the measurement results described below represent a response of the entire 16-element array being driven simultaneously (not including the power FET's). Digital measurements were performed by modulating the circuit input using a 150-ps rise time source, and measuring the output using a digitizing scope. Fig. 7 shows a plot of a typical measured response (solid line), yielding a rise time of 2.87 ns for a circuit biased to an optimum operating point. The correlation between the optical

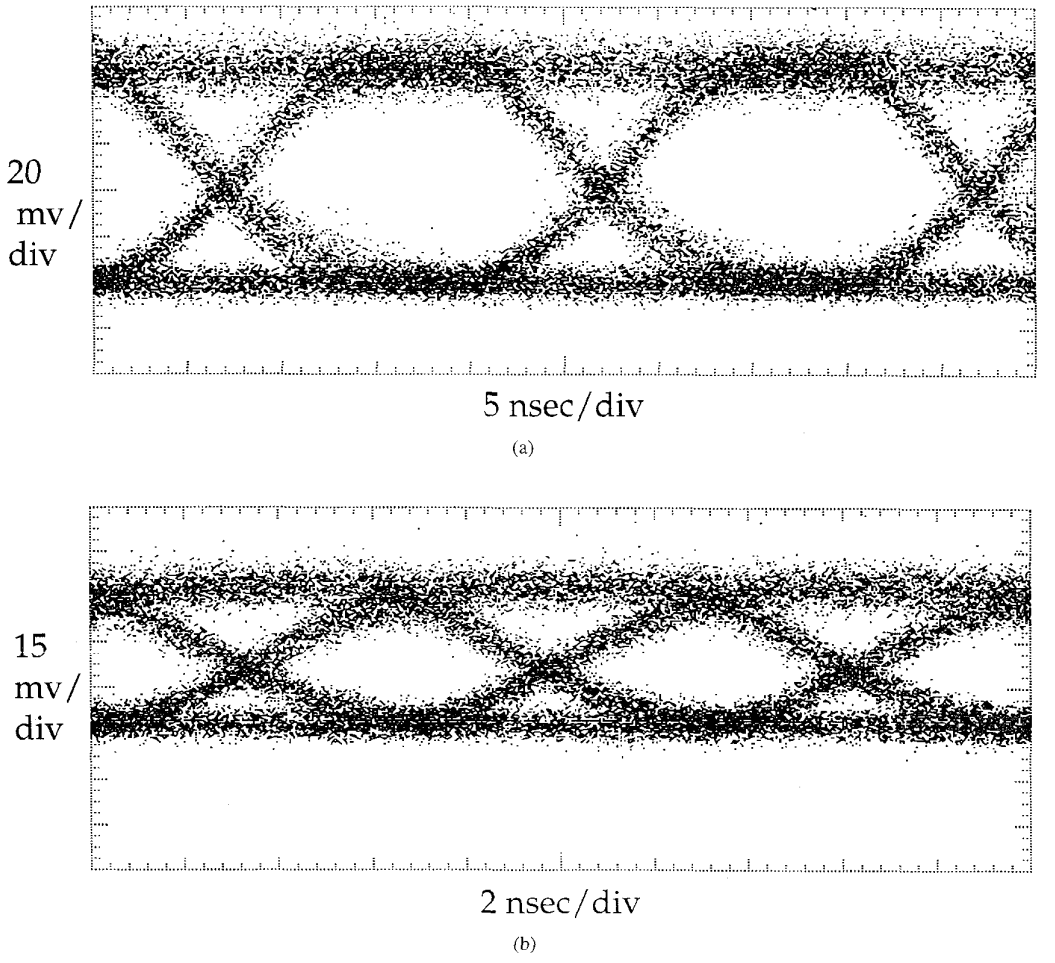

Fig. 10. Eye diagrams of one of the optical channels operating at (a) 50 Mb/s and (b) 155 Mb/s, respectively.

measurements and the electrical measurements is very good. Also shown in Fig. 7 is the model-predicted rise time of 0.99 ns.

S-parameter measurements on the array were also performed using a 5-KHz–3.0-GHz network analyzer. In order to de-embed the circuit performance from the combined circuit-plus-package performance, the network analyzer was calibrated using a modified QFP/PCB calibration package. The calibration package contained a 50-Ω termination, a short-circuit termination, an open-circuit termination, and a straight-through connection. A complete set of S parameters was taken on five of the 16 channels, and this data was used to calculate the properties of the circuit including the current gain, h_{21}. In addition, the data was used to measure the array uniformity. Fig. 8(a) shows a plot of the measured circuit current gain h_{21} for five of the channels. From these measurements, we found the average $f_t = 440$ MHz. The data oscillates over the first 400 MHz. Based on the care taken in calibrating the network analyzer, we are confident these oscillations were not due to improper impedance matching to the network analyzer; the input and output impedances were matched to 50 and 100 Ωs, respectively. Using the above models, the predicted h_{21} (solid) is also shown in Fig. 8(b), with a predicted $f_t = 691$ MHz. As is expected based on the above digital measurements, the agreement between measured and predicted f_t is off by a factor of approximately 1.57.

VII. Board-to-Board Optical Interconnection

A simple board-to-board optical interconnection was constructed using the two-sided optical backplane approach shown in Fig. 9. The optomechanics were based on a slotted baseplate approach [21]. Light from a Ti:Sapphire laser was delivered to the baseplate and collimated using a single-mode fiber and collimating optics. A binary phase grating was used to generate an 8×4 spot array to illuminate the modulators. The beam steering was done using a quarterwave plate/polarizing beamsplitter (QWP/PBS) combination. Vertically polarized light was directed onto the transmitter and then circularized after one pass through the quarterwave plate. Digital data was encoded on the optical beams via the modulator and transmitted through the QWP/PBS assembly to the receiver board. The signal beam was detected, demodulated, and the digital data was recovered, this data being driven off-chip to the PCB outputs. Fig. 10(a) and (b) show eye diagrams of one of the channels operating at 50 Mb/s and 155 Mb/s, respectively. The data reflects open eyes and good fidelity at

theses data rates. The rise times are not as fast as the rise time measured by directly modulating the receiver, however, this is to be expected based on the fact that they are being driven by a source with only a 3-dB (2-to-1) contrast ratio.

VIII. Conclusion

We have described the design, modeling, and characterization of FET-SEED transceiver arrays. Models were developed which accurately predict the experimentally measured performance of 2-D transceiver arrays. These data provide a measure of the present state of FET-SEED technology. Finally, these transceivers were used to demonstrate a simple unidirectional board-to-board optical interconnect capable of operating at 155Mb/s. This demonstration highlights the potential impact this technology could have in providing 2-D optical data links for PCB-to-PCB communication within a backplane.

Acknowledgment

The authors gratefully acknowledge W. M. Robertson of the Institute of Information Technology, National Research Council of Canada, for providing the binary phase grating used in the optical interconnect.

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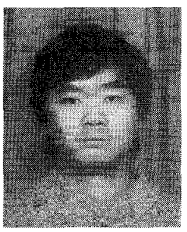
David V. Plant (S'86–M'89) was born in 1962 in Vancouver, Canada. He received the B.S., M.S., and Ph.D. degrees from Brown University in 1985, 1986, and 1989, respectively.

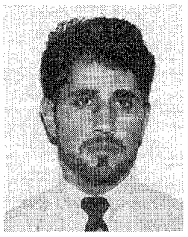
From 1989–1993, he was a Research Engineer in the Department of Electrical Engineering at the University of California at Los Angeles. In 1993, he joined the Department of Electrical Engineering at McGill University, Montreal, Canada, as an Assistant Professor. His research interests include optoelectronic devices and packaging, optical interconnects, and free-space digital optics.

Dr. Plant is a member of the Optical Society of America and the American Physical Society and is on the technical program committees for the 1996 IEEE Summer Topical Meeting on Smart Pixels and the 1996 LEOS Annual Meeting.



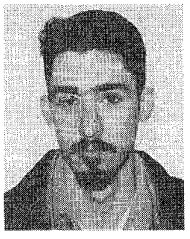
Alain Z. Shang was born in Brussels, Belgium, on June 3, 1968. He received the B.Eng. degree in electrical engineering from Concordia University, Montreal, Canada, in 1990 and the M.Eng. degree in electrical engineering from McGill University, Montreal, Canada, in 1992. He is currently a candidate for the Ph.D. degree at McGill University

In 1992, he was a Junior Research Officer at the National Research Council of Canada. In 1992–1993, he was a Visiting Researcher at the Electronic Research Laboratory (ERL) of the University of California at Berkeley. His research interests include optical VLSI interconnects, smart pixel design, and optoelectronic packaging.



Marcos R. Otazo was born on December 16, 1970, in La Paz, Bolivia. He received the B.Sc. degree in engineering physics from Queen's University, Kingston, Canada, in 1993 and the M.Eng. degree in electrical engineering from McGill University, Montreal, Canada, in 1996.

His research interests, while at McGill University, were in the area of optoelectronic packaging for photonic system applications. At present, he is with Northern Telecom, Ltd., Montreal, Canada.



David R. Rolston was born on January 16, 1971, in Ottawa, Canada. He received the bachelor's degree with honors in electrical engineering from McGill University, Montreal, Canada, in 1993. He is currently a candidate for the Ph.D. degree at McGill University.

He has been working on several aspects of the design and development of photonic backplanes involving free-space optics. He has had two primary fields of concentration since beginning his Ph.D. work. The first was an analysis of a high-density optical interconnection scheme using a clustered window approach for relaying multiple beams through single diffractive lenslets. The second is the design, layout, fabrication, and testing of CMOS silicon smart pixel arrays with solder-bump bonded MQW receivers and modulators developed by AT&T. The smart pixel arrays have been based on the Hyperplane architecture for switching and packet routing systems.

Brian Robertson received the Ph.D. degree in physics from Heriot-Watt University, Scotland, in 1993.

During the course of his Ph.D. work, he carried out research in the design, fabrication, and analysis of dichromated gelatin (DCG) volume holographic optical elements. Since 1993, he has been a Member of the Photonic Systems Group at McGill University, carrying out research in the fields of optical interconnect design, optomechanics, optical alignment, and free-space photonic backplane technology.

Dr. Robertson is a member of the Optical Society of American and OptoScot.

H. Scott Hinton (S'81–M'82–SM'92) was born in Salt Lake City, UT, in 1951. He received the B.S.E.E. degree from Brigham Young University, Provo, UT, in 1981 and the M.S.E.E. degree from Purdue University, Lafayette, IN, in 1982.

In 1981, he joined AT&T Bell Laboratories, Naperville, IL, as a Member of the Technical Staff. He was promoted to Supervisor of the Photonic Switching Technologies group in 1985 and then Head of the Photonic Switching Department in 1989, where his department was responsible for the development of systems applications of the S-SEED and FET-SEED technology. From 1992 to 1994, he was the BNR-NT/NSERC Chair in Photonic Systems at McGill University. In 1994, he accepted the position as the Hudson Moore, Jr., Professor of Electrical and Computer Engineering at the University of Colorado at Boulder. His current research is focused on developing systems applications of smart pixels and free-space optical interconnection.

Mr. Hinton was an IEEE LEOS Distinguished Lecturer for 1993–1994 and is a member of the Optical Society of America.