TECHNICAL NOTE

4 × 4 vertical-cavity surface-emitting laser (VCSEL) and metal–semiconductor–metal (MSM) optical backplane demonstrator system

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We describe a system demonstrator based on vertical-cavity surface-emitting lasers, metal–semiconductor–metal detectors, printed circuit board (PCB) level optoelectronic device packaging, a compact bulk optical relay, and novel barrel/PCB optomechanics. The entire system was constructed in a standard VME electrical backplane chassis and was capable of operating at >1.7 Gbit/s of aggregate data capacity. In addition to the component technologies developed, we describe operational testing and characterization of the demonstrator. © 1996 Optical Society of America

Future digital systems such as asynchronous transfer mode (ATM) switching systems and massively parallel processing computer systems will have large printed circuit board (PCB)-to-PCB connectivity requirements to support the large aggregate throughput demands placed on such systems. Current electronic technology may not be capable of supporting both the connection densities and the bandwidth required because of the limitations of multipoint electrical connections over backplane distances.[1] Two-dimensional, free-space optical interconnects represent a potential solution to the needs of these connection-intensive digital systems. When implemented at the PCB-to-PCB level in the form of an optical backplane, this technology is potentially capable of providing greater connectivity at higher data rates than can be supported by current or projected electronic backplanes. The identification of critical issues in free-space optical backplanes is being pursued in the form of system demonstrator experiments.[2–6] We describe a system demonstrator based on vertical cavity surface emitting lasers (VCSEL's), metal semiconductor metal (MSM) detectors, PCB level optoelectronic device packaging, a compact bulk optical relay, and novel barrel–PCB optomechanics. The entire system was constructed with a standard VME electrical backplane chassis and operated at >1.7 Gbits/s of aggregate data flow. In addition to the component technologies developed, we describe operational testing and characterization of the demonstrator.

Figure 1 shows the demonstration system. Based on the benefits arising from decoupling the alignment of optoelectronic device arrays from the PCB's in a backplane system (these PCB's must undergo insertion and extraction cycles), the approach taken for this system was that of mechanically decoupling the switching nodes or processor boards from the optical interconnect layer. This approach resulted in the concept of motherboards (MB's) that resided in a conventional manner inside the VME chassis and daughterboards (DB's) that were part of the optical interconnect layer.

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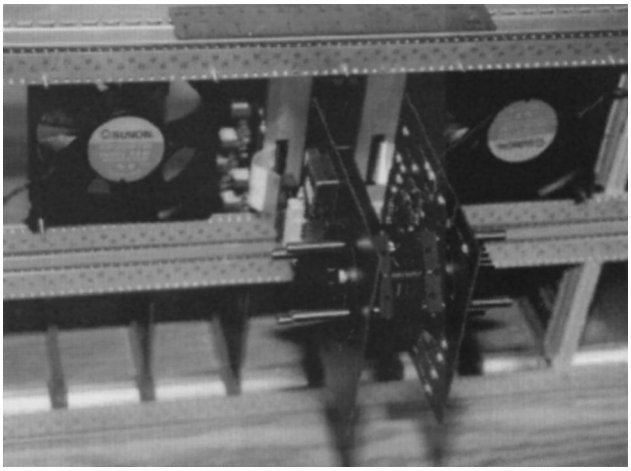

Fig. 1. VCSEL–MSM daughter boards interconnected with rod and barrel optomechanics.

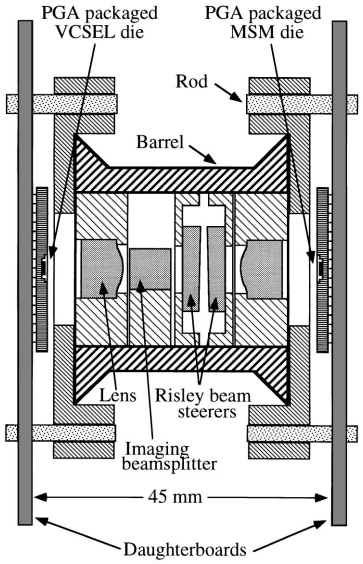

Fig. 2. Schematic of the rod and barrel optomechanics and the associated optics used for the free-space optical interconnect.

Because the requirement of connectivity into or out of the backplane is a fraction of the information traversing the backplane[7,8] and because the length of the point-to-point interconnect between the MB and the DB was small, a scalable high-speed flexible 50-Ω connector was chosen to connect the MB's and the DB's. In addition to optomechanical advantages the DB provided the first- and second-level packaging for the smart pixels and their associated support electronics. The two-dimensional device arrays used to provide the optical link between the DB's were VCSEL's for the transmitter and MSM's for the receiver. The light was relayed from the VCSEL plane to the MSM plane through a symmetric telecentric imaging system with external viewing capabilities.

The transmitter DB included a 4×4, 850-nm VCSEL array (VIXEL Corporation, Model LA-1-850 with a device pitch of 125 μm) packaged in a pin grid array (PGA) chip carrier. The PCB level packaging of the PGA was accomplished with custom, impedance-controlled, four-layer PCB's. In addition, a thermo-electric (TE) cooler was mounted on the back of the PGA to allow for active cooling of the VCSEL array. This was accomplished by leaving a hole in the VCSEL DB. To avoid the problem of slow drive electronics, each individual VCSEL was operated through a dedicated bias tee mounted on the MB. On the receiver DB, a 4×4 MSM array with 50-μm windows (fabricated by McMaster University) was hybridly packaged in a 68-pin PGA with commercially available Hewlett Packard silicon millimeter wave monolithic integrated circuit (MMIC) transimpedance amplifier chips. To minimize long leads and unwanted inductive parasitics, the transimpedance amplifier chips were mounted directly into the PGA cavity adjacent to the detector array chip. The output of each MSM was wire bonded to an amplifier chip. The outputs of the transimpedance amplifier chips were then wire bonded to the PGA outputs. These amplifier outputs were fed into variable gain amplifiers that were surface mounted on the receiver DB and configured as limiting amplifiers to achieve emitter-coupled logic (ECL) voltage levels. In both cases the DB's were connected to the MB's through the high-speed connectors.

The optical interconnect consisted of a symmetric telecentric imaging system that employed two inexpensive injection-molded glass aspherical lenses ($f =$ 6.24 mm). Risley beam steerers were used for fine adjustment of the optical beams, and a 4-mm beamsplitter cube was used to provide a view port. Figure 2 shows a schematic of the optics and optomechanics. The objective of this approach was to design and build a compact, low-cost, stable, and rapidly assembled optomechanical support structure that could be integrated into an industry standard (VME) 6U chassis. The physical separation between two DB's was 45 mm. The barrel had two 45° bevels, one on each side. These bevels supported the DB barrel adapters that acted as an interface between the DB's and the optomechanical components. The barrel itself was fixed in position relative to the VME chassis, and the optomechanical interface permitted motion of the DB's relative to the barrel. The utility of a flexible connector between the DB's and the MB's was key because the DB's were required to move independently relative to the chassis. Neither the die-to-package nor the package-to-board alignment tolerances was critical to the alignment of the system because the DB optomechanics were designed to compensate for these misalignments. During assembly, the optomechanics allowed signal beams generated by the VCSEL array to be positioned to within 50 μm of their required location. Fine alignment was provided by the Risley steerers, which had a range of 80 μm and a resolution of 1 μm. Finally, in addition to TE cooling the optoelectronics, two cooling fans were bolted to the VME chassis support spine as is shown in Fig. 1. This spine also supported the rod and barrel optomechanics; thus the fans were directly me-

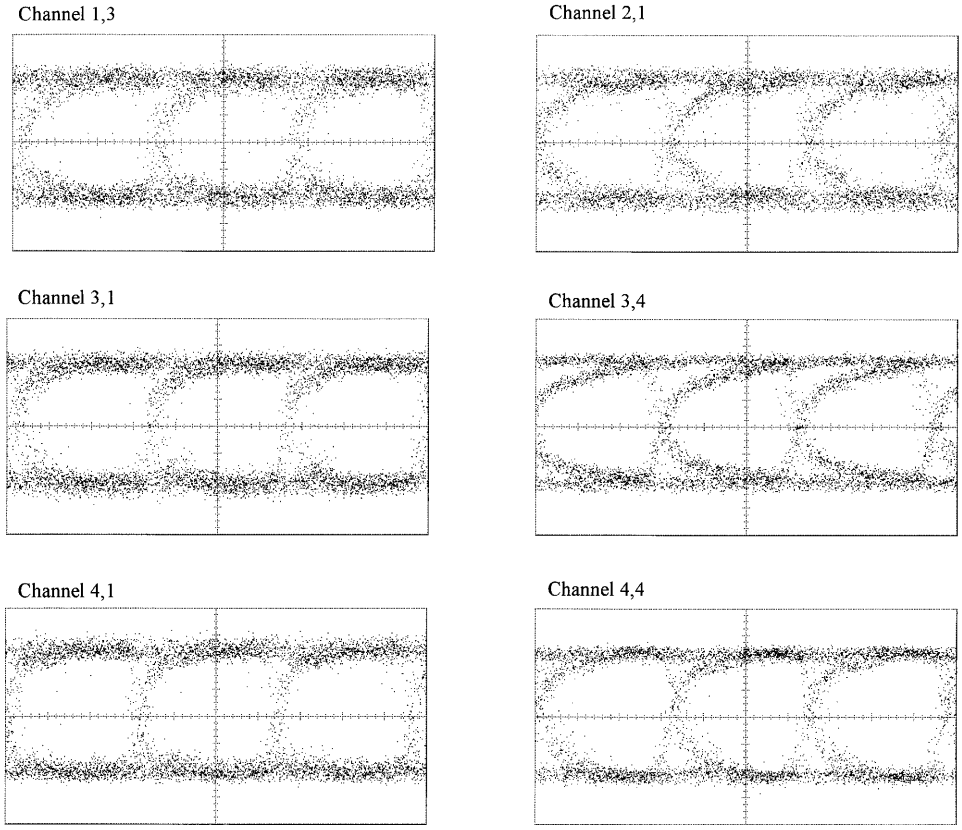

Fig. 3. Six of the 16 channels operating at 155 Mbits/s (0.4 V and 20 ns full scale).

chanically coupled to the interconnect. These fans blew air directly onto the DB's and provided an additional heat-removal mechanism. During all the operational testing described below, not only was the VME chassis freestanding but also the two cooling fans were on at all times.

The system was operated in a number of different modes. Initially, each of the 16 channels was individually operated with data rates as fast as 500 Mbits/s on the best channels. Figure 3 shows eye diagrams of six of the channels operating at 155 Mbits/s. In the parallel mode of operation 11 channels could be operated simultaneously. In this mode these 11 channels were operated at 155 Mbits/s with $<$2-ns edges and high signal quality. This represented a greater than 1.7 Gbits/s of aggregate data flow. The stability and robustness of the system were excellent. The mechanical stability of the system was monitored for a period of 21 days. During that time the transverse (x, y) misalignment was measured to be less than 2 μm. In addition, the system also was tested under MB insertion and extraction, showing no misalignment after more than 30 insertion and extraction cycles. Finally, both the introduction of mechanically coupled fans to the chassis and shock on the DB's showed no effect on the alignment of the system.

In conclusion, we have constructed and tested a VCSEL–MSM optical backplane demonstration system capable of $>$1.7 Gbits/s of aggregate data capacity with as fast as 500-Mbits/s operation on individual channels. The effective connection density of the system is $>$6000 channels/cm^2. With custom rod and barrel optomechanics and a DB–MB assembly, the system demonstrated excellent robustness and stability. This demonstration system points to the utility of using free-space digital optics to achieve PCB-to-PCB interconnection. Future demonstrators will expand on these results by implementing sophisticated architectures such as the HyperPlane that utilizes the increased connectivity provided by an optical backplane.[5,6]

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